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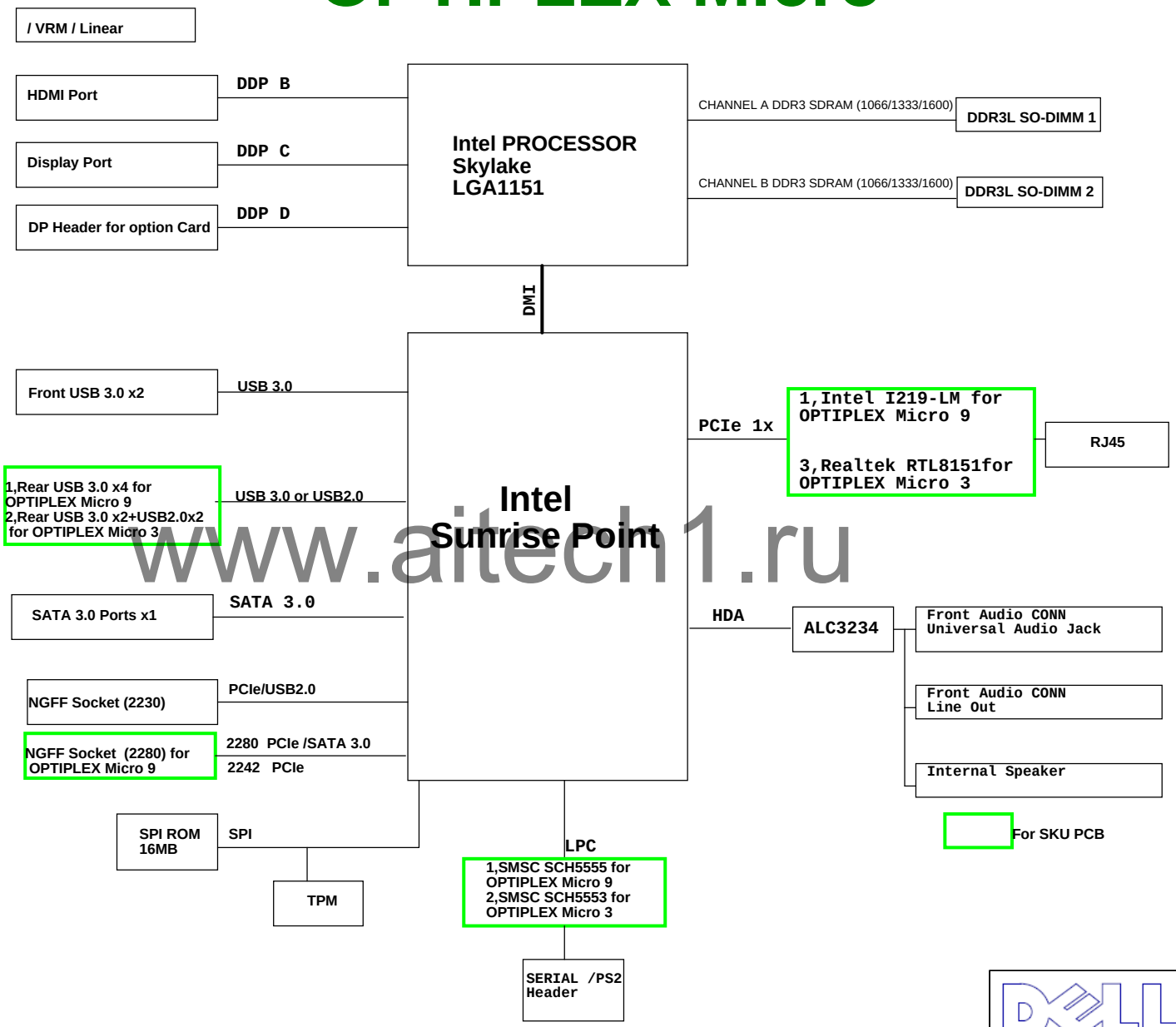

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Title: **Index / Block diagram**

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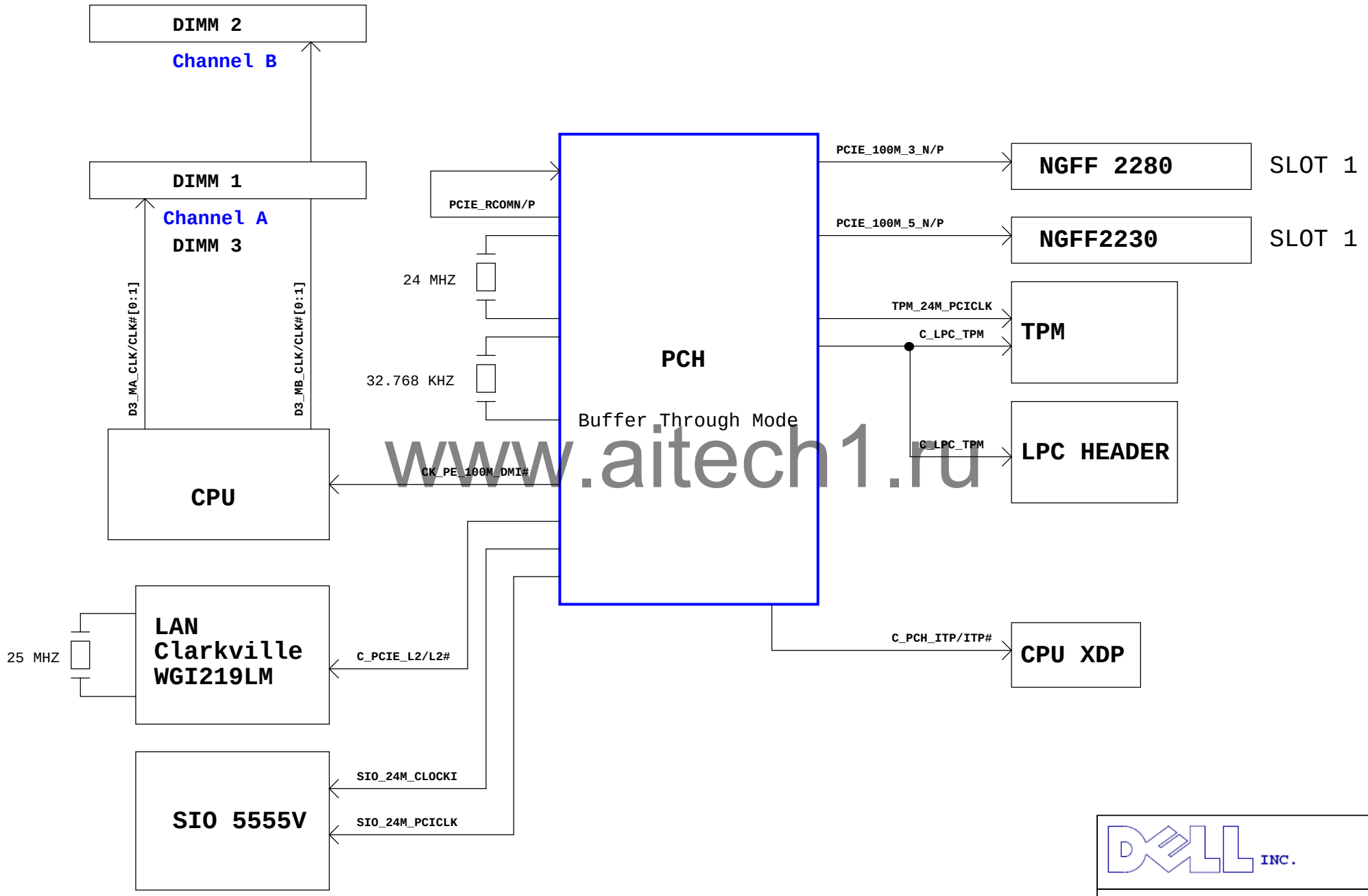

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Clock Distribution

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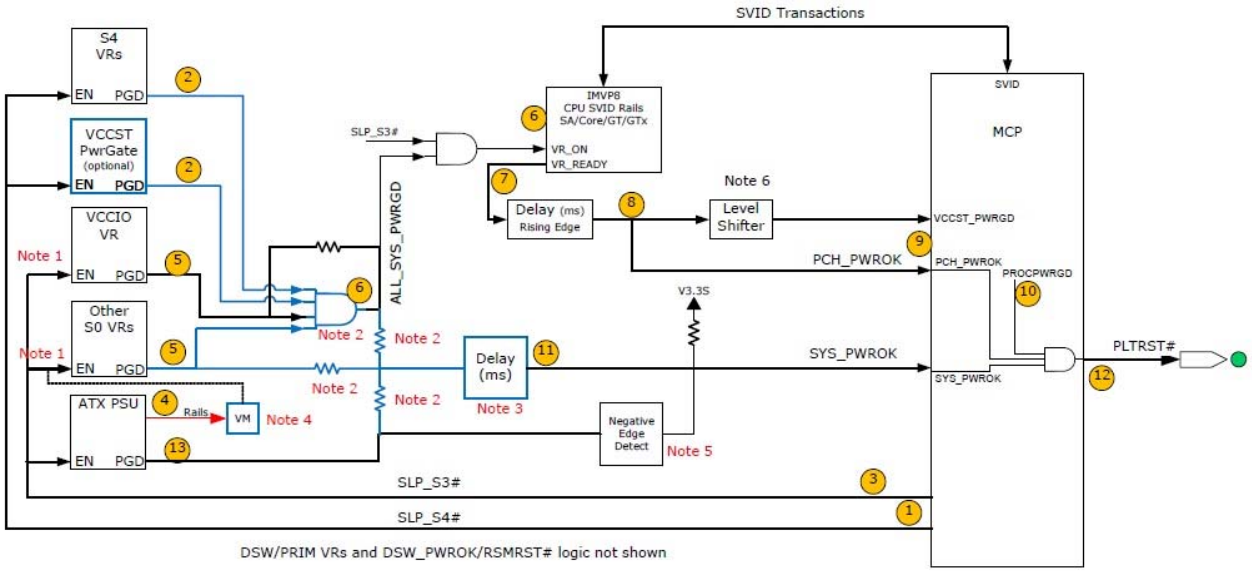

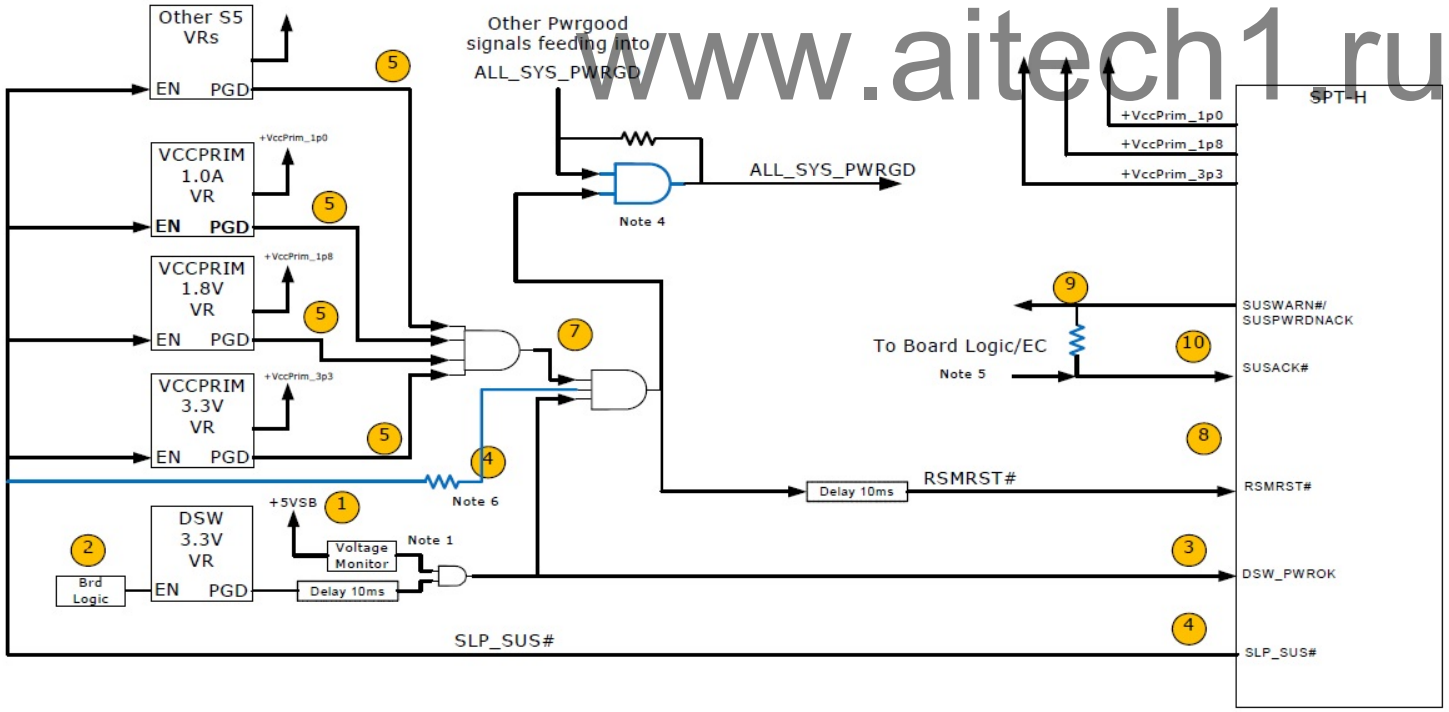

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Title

Reset / Power Good Map

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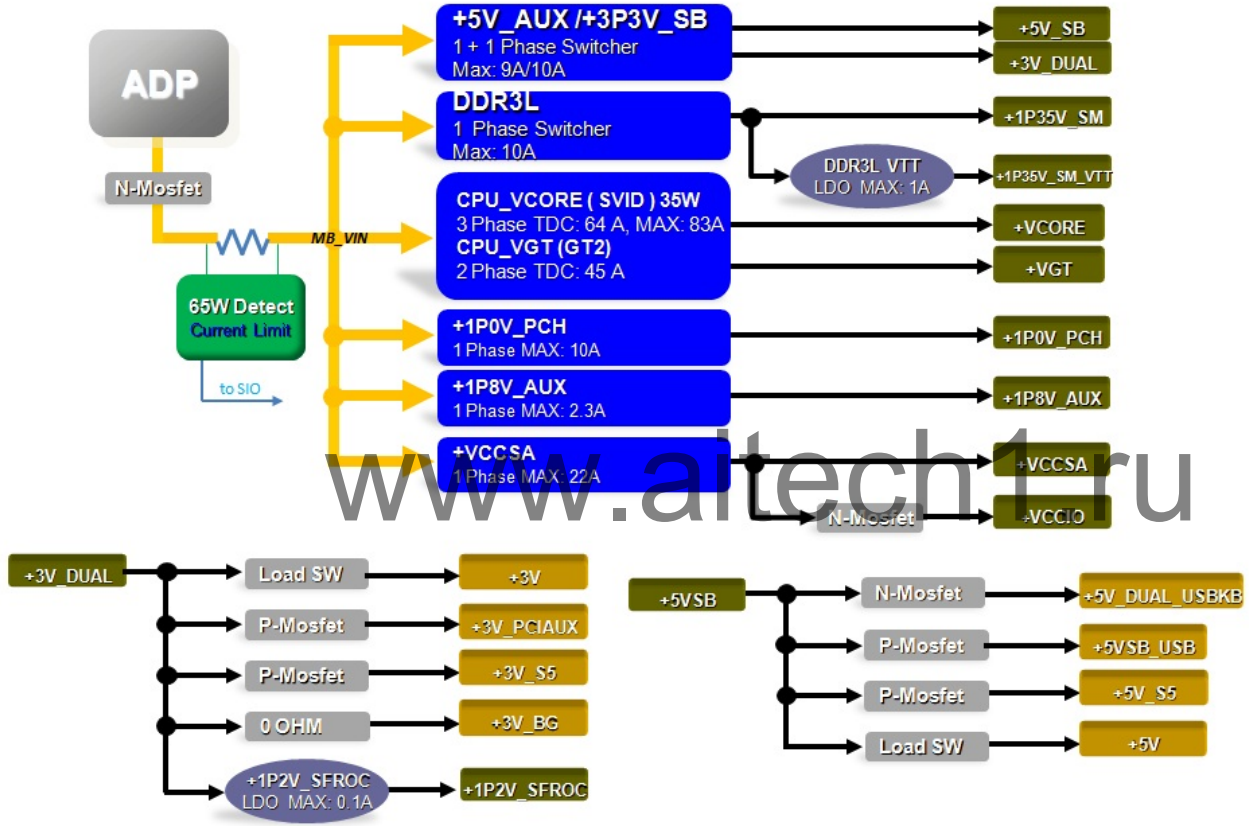
POWER DELIVERY MAP

Power Delivery Map



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Title: **Power Delivery Map**

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PIN OUT	Power well	Bufffer Type	Signal Name	EX-PU/PD	*Current Usage I/O/NU/Native/Strapping	Programming Function
4	V3_S5	IO4	NC	NA	Native	N/A
5	V3_S5	IO4	NC	NA	Native	N/A
7	V3_S5	IO4	NC	NA	Native	N/A
8	V3_S5	IO4	NC	NA	Native	N/A
70	V3_S5	IO4	S_SUSWARN#	NA	Native	N/A
22	V3_S5	IO4	O_PECI_REQ#	10k pull-up to +3V	Native	N/A
25	V3_S5	IO8	O_YELLOW#	499 pull-up to +5V_S5	Native	N/A
26	V3_S5	IO8	O_GREEN#	499 pull-up to +5V_S5	Native	N/A
27	V3_S5	IO8	S_SML1DATA	2.2k pull-up to +3V_S5	Native	N/A
28	V3_S5	IO8	S_SML1CLK	2.2k pull-up to +3V_S5	Native	N/A
30	V3_S5	IO4	O_DPWROK	10k pull-down to GND	Native	N/A
35	V3_S5	IO4	TMIN_SHIFT	8.2k pull-up to +3V_S5 330k pull-down to GND (Dummy)	I	1 : default 0 : Tmin down adjustment
36	V3_S5	IO4	O_PWRBTN#IN	1k pull-up to +3V_DUAL (Dummy)	Native	N/A
38	V3_S5	LVIOD24	H_PROCHOT#	51ohm pull-up to H_CPU_VCCIO_RIGHT	Native	N/A
39	V3_S5	IO4	O_SEN_CPUFAN	1k pull-up to +3V	Native	N/A
40	V3_S5	IO4	O_SEN_CHAFAN	1k pull-up to +3V	Native	N/A
41	V3_S5	IO4	NC	NA	NU	N/A
49	V3_S5	IO4	O_CPUFAN_PWM	4.7k pull-up to +3V	Native	N/A
50	V3_S5	IO4	O_CHAFAN_PWM	4.7k pull-up to +3V	Native	N/A
51	V3_S5	IO4	NC	NA	NU	N/A
52	V3_S5	IO4	O_FP_CBL_DET#	8.2k pull-up to +3V_S5	I	1 : default 0 : power switch cable plugged
53	V3_S5	IO4	X_PLTRST_PCIE_SLOT#	NA	Native	N/A
54	V3_S5	IO4	NC	NA	NU	N/A
55	V3_S5	OD4	O_PSON#	4.7k pull-up to +5VSB	Native	N/A
56	V3_S5	IO4	O_AUD_PCSPKR_DET#	8.2k pull-up to +3V_S5	I	1 : default 0 : PC speaker cable plugged
58	V3_S5	IO4	O_SUS_3V_F_ON	NA	Native	N/A
59	V3_S5	IO4	PWRGD_3V	NA	Native	N/A
60	V3_S5	O4	O_RSMRST#	NA	NU	N/A
69	V3_S5	IO4	NC	NA	NU	N/A
72	V3_S5	IO8	NC	NA	NU	N/A
74	V3_S5	IO8	NC	NA	NU	N/A
77	V3_S5	IO4	O_PME#	10k pull-up to +3V_S5	Native	N/A
78	V3_S5	IO4	NC	NA	NU	N/A
98	V3_S5	IO4	O_DCD1#_R	NA	Native	N/A
99	V3_S5	IO4	O_DSR1#_R	NA	Native	N/A
100	V3_S5	IO4	O_RXD1_R	NA	Native	N/A
101	V3_S5	IO4	O_RTS1#_R	10k pull-up to +3V	Native	N/A
102	V3_S5	IO8	O_TXD1_R_C	10k pull-up to +3V	Native	N/A
103	V3_S5	IO4	O_CTS1#_R	NA	Native	N/A
104	V3_S5	IO4	O_DTR1#_R	NA	Native	N/A
105	V3_S5	IO4	O_RI1#_R	NA	Native	N/A
107	V3_S5	IO4	NC	NA	Native	N/A
108	V3_S5	IO4	NC	NA	Native	N/A
109	V3_S5	IO4	NC	NA	Native	N/A
110	V3_S5	IO4	O_PWR2_PRSNT	10k pull-up to +3V	Native	N/A
111	V3_S5	IO8	O_MB_REG_PG	10k pull-up to +3V	Native	N/A
112	V3_S5	IO4	NC	NA	Native	N/A
113	V3_S5	IO4	O_MEM_REG_PG	10k pull-up to +3V	Native	N/A
114	V3_S5	IO4	NC	NA	Native	N/A
120	V3_S5	IO4	O_KB_RST#	10k pull-up to +3V	Native	N/A
121	V3_S5	IO4	O_A20GATE	10k pull-up to +3V	Native	N/A
124	V3_S5	IO4	S_SLP_S5#	NA	Native	N/A
127	V3_S5	IO4	O_SPEAKER	8.2k pull-up to +3V_S5(dummy) 8.2k pull-down to GND	Native	N/A
128	V3_S5	IO4	S_SLP_M#	NA	Native	N/A
75	V3_S5	IO4	O_SUS_5VON	22k pull-up to +5VSB	Native	N/A
76	V3_S5	IO4	O_SUS_3V_ON	NA	Native	N/A
84	V3_S5	IO12	NC	NA	Native	N/A
85	V3_S5	IO12	NC	NA	Native	N/A
86	V3_S5	IO12	NC	NA	Native	N/A
87	V3_S5	IO12	NC	NA	Native	N/A
88	V3_S5	IO12	NC	NA	Native	N/A
89	V3_S5	IO12	NC	NA	Native	N/A
90	V3_S5	IO12	NC	NA	Native	N/A
91	V3_S5	IO12	NC	NA	Native	N/A
63	V3_S5	IO4	NC	NA	Native	N/A
64	V3_S5	IO4	NC	NA	Native	N/A
65	V3_S5	IO4	NC	NA	Native	N/A
66	V3_S5	IO4	NC	NA	Native	N/A
97	V3_S5	IO12	NC	NA	Native	N/A
15	V3_S5	IO4	NC	NA	Native	N/A
80	V3_S5	IO8	S_SMBDATA_RESUME	2.2k pull-up to +3V_S5	Native	N/A
81	V3_S5	IO8	S_SMBDATA_MAIN	2.7k pull-up to +3V	Native	N/A
82	V3_S5	IO8	S_SMBCLK_RESUME	2.2k pull-up to +3V_S5	Native	N/A
83	V3_S5	IO8	S_SMBCLK_MAIN	2.7k pull-up to +3V	Native	N/A
93	V3_S5	IO8	O_PCIAUX_CTRL	NA	Native	N/A
94	V3_S5	IO8	O_PCIAUX_GATE	NA	NU	N/A
95	V3_S5	IO4	NC	NA	Native	N/A
96	V3_S5	IO12	O_SUS_ACK_EN#	NA	NU	N/A

PCH GPIO Summary

GPIO	Mult Function Pin	PIN OUT	Type	Power Well	Default	Signal Name	IN-PU/PD	EX-PU/PD	*Current Usage
GPIO[0]	BMBUSY#/GPIO0	G38	I/O	Core	GPI	S_PECI_REQ#	--	10k pull-up to +3V	I
GPIO[1]	TACH1/GPIO1	AT31	I/O	Core	GPI	S_GPI_CHASSIS_ID0	20K IN-PU (only on TACH1)	10k pull-up to +3V 1k pull-down to GND (dummy)	I
GPIO[2]	PIRQE#/GPIO2	AR30	I/OD	Core	GPI	PCIE_MINI_CPUSB_DETECT#	--	8.2k pull-up to +3V	I
GPIO[3]	PIRQF#/GPIO3	AV29	I/OD	Core	GPI	V_DDSP_C_HPD	--	---	I
GPIO[4]	PIRQG#/GPIO4	AV28	I/OD	Core	GPI	V_GPI_VGA_CBL_DET#	--	8.2k pull-up to +3V	I
GPIO[5]	PIRQH#/GPIO5	AT27	I/OD	Core	GPI	PCIE_MINI_CPPE_DETECT#	--	8.2k pull-up to +3V	I
GPIO[6]	TACH2/GPIO6	AM28	I/O	Core	GPI	S_GPIO6	20K IN-PU (only on TACH2)	10k pull-up to +3V	NU
GPIO[7]	TACH3/GPIO7	AV34	I/O	Core	GPI	S_GPI_SKU2	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[8]	GPIO8	AC40	I/O	Suspend	GPO	S_IGC_EN_N	20K IN-PU	---	NU (connected to XDP_PCH)
GPIO[9]	OC5#/GPIO9	AC41	I/O	Suspend	Native	X_WLAN_WAKE#	--	8.2k pull-up to +3V_S5	I
GPIO[10]	OC6#/GPIO10	AF40	I/O	Suspend	Native	U_USB_OC_R_#6	--	---	Native
GPIO[11]	SMBALERT#/GPIO11	AG31	I/O	Suspend	Native	X4_WAKE#	--	10k pull-up to +3V_S5	NU
GPIO[12]	LAN_PHY_PWR_CTRL/GPIO12	AL48	I/O	Suspend	Native	L_LAN_DISABLE#	--	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	O
GPIO[13]	GPIO13	AN22	I/O	Suspend	GPI	S_GPIO13	--	10k pull-up to +3V_S5	NU
GPIO[14]	OC7#/GPIO14	AG40	I/O	Suspend	Native	U_USB_OC_R_#7	--	---	Native
GPIO[15]	GPIO15	AE34	I/O	Suspend	GPO	S_GPIO15	--	10k pull-up to +3V_S5	NU
GPIO[16]	SATA4GP/GPIO16	M39	I/O	Core	GPI	S_SATA4GP	--	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[17]	TACH0/GPIO17	AP28	I/O	Core	GPI	S_GPI_CHASSIS_ID1	20K IN-PU (only on TACH0)	10k pull-up to +3V 1k pull-down to GND(dummy)	I
GPIO[18]	PCIECLKRQ1#/GPIO18	P39	I/O	Core	Native	S_GPIO18	--	10k pull-up to +3V	NU (connected to XDP_PCH)
GPIO[19]	SATA1GP/GPIO19	J40	I/O	Core	GPI	S_SATA1GP	20K IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO[20]	PCIECLKRQ2#/GPIO20	P37	I/O	Core	Native	S_SMI_N	--	10k pull-up to +3V 10k pull-down to GND (dummy)	NU (connected to XDP_PCH)
GPIO[21]	SATA0GP/GPIO21	M37	I/O	Core	GPI	S_GPI_BRD_REV0	--	10k pull-up to +3V (dummy) 10k pull-down to GND	I
GPIO[22]	SCLOCK/GPIO22	[illegible]	I/O	Core	GPI	S_PCH_CONFIG_JUMPER	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	NU
GPIO[23]	LDRQ1#/GPIO23	AK26	I/O	Core	Native	S_LDRQ1#	20K IN-PU	--	NU
GPIO[24]	GPIO24	AE34	I/O	Suspend	GPO	H_SKTOCC#	--	100k pull-up to +3V_S5	I
GPIO[25]	PCIECLKRQ3#GPIO25	AA39	I/O	Suspend	Native	S_GPIO25	--	100k pull-up to +3V_S5	NU
GPIO[26]	PCIECLKRQ3#GPIO26	W35	I/O	Suspend	Native	S_MFG_MODE_OR	--	10k pull-up to +3V_S5	O
GPIO[27]	GPIO27	AU34	I/O	Deep Sleep	GPI	L_LAN_WAKE_N	20K IN-PU	4.7k pull-up to +3V_DUAL	I
GPIO[28]	GPIO28	V41	I/O	Suspend	GPO	S_GPIO28	--	10k pull-up to +3V_S5	NU
GPIO[29]	SLP_WLAN#/GPIO29	AL39	I/O	Suspend	GPI	S_GPIO29	--	10k pull-up to +3V_S5	NU
GPIO[30]	SUSWARN#/SUSPWRDNACK /GPIO30	AG41	I/O	Suspend	Native	S_SUSWARN#	--	--	Native
GPIO[31]	GPIO31	AM36	I/O	Deep Sleep	GPI	S_PSWD_CLR	20K IN-PD	8.2k pull-up to +3V_DUAL	I
GPIO[32]	CLKRUN#/GPIO32	N32	I/O	Core	GPO	S_GPI_SKU0	--	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[33]	HDA_DOCK_EN#/GPIO33	AV26	I/O	Core	GPO	S_GPIO33	PD	--	NU
GPIO[34]	GPIO34	N34	I/O	Core	GPI	S_GPIO34	--	10k pull-up to +3V	NU
GPIO[35]	GPIO35	M40	I/O	Core	GPO	S_GPI_SKU1	--	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[36]	SATA2GP/GPIO36	H40	I/O	Core	GPI	S_GPIO36	20K IN-PD	1k pull-up to +3V (dummy) 10k pull-down to GND (dummy)	Strapping
GPIO[37]	SATA3GP/GPIO37	N41	I/O	Core	GPI	S_GPIO37	20K IN-PD	1k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[38]	SLOAD/GPIO38	H41	I/O	Core	GPI	S_GPI_CHASSIS_ID2	--	10k pull-up to +3V (dummy) 10k pull-down to GND	I
GPIO[39]	SDATAOUT0/GPIO39	R31	I/O	Core	GPI	A_FP_PRES#	--	10k pull-up to +3V	I
GPIO[40]	OC1#/GPIO40	AF37	I/O	Suspend	Native	U_USB_OC_R_#1	--	8.2k pull-up to +3V_S5	NU
GPIO[41]	OC2#/GPIO41	AD39	I/O	Suspend	Native	U_USB_OC_R_#2	--		Native
GPIO[42]	OC3#/GPIO42	AD40	I/O	Suspend	Native	U_USB_OC_R_#3	--		Native
GPIO[43]	OC4#/GPIO43	AF39	I/O	Suspend	Native	U_USB_OC_R_#4	--		Native
GPIO[44]	PCIECLKRQ5#/GPIO44	AA36	I/O	Suspend	Native	S_INTRUD_CBL_DET#	20K IN-PU	10k pull-up to +3V_S5	I
GPIO[45]	PCIECLKRQ6#/GPIO45	W32	I/O	Suspend	Native	S_GPIO45	--	10k pull-up to +3V_S5	NU
GPIO[46]	PCIECLKRQ7#/GPIO46	AA40	I/O	Suspend	Native	S_GPI_BRD_REV1	20K IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	I
GPIO[48]	SDATAOUT1/GPIO48	L40	I/O	Core	GPI	V_DDSP_B_HPD	--	---	I
GPIO[49]	SATA5GP/GPIO49	N40	I/O	Core	GPI	S_GPIO49	--	10k pull-up to +3V (dummy)	Strapping
GPIO[50]	GPIO50	AH26	I/O	Core	GPI	S_GPIO50	--	10k pull-up to +3V	NU
GPIO[51]	GPIO51	AU31	I/O	Core	GPO	S_GPIO51	20K IN-PU	1k pull-up to +3V (dummy) 10k pull-down to GND	Strapping
GPIO[52]	GPIO52	AJ26	I/O	Core	GPI	S_GPIO52	--	10k pull-up to +3V	NU
GPIO[53]	GPIO53	AV31	I/O	Core	GPO	S_GPIO53	20K IN-PU	1k pull-down to GND (dumm	Strapping
GPIO[54]	GPIO54	AW33	I/O	Core	GPI	S_GPIO54	--	10k pull-up to +3V	NU
GPIO[55]	GPIO55	R30	I/O	Core	GPO	S_GPIO55	20K IN-PU	4.7k pull-down to GND (dummy	Strapping
GPIO[57]	GPIO57	AC36	I/O	Suspend	GPI	S_GPIO57	--	10k pull-up to +3V_S5	NU
GPIO[58]	SML1CLK/GPIO58	AK36	I/O	Suspend	Native	S_SML1CLK	--	2.2k pull-up to +3V_S5	Native
GPIO[59]	OC0#/GPIO59	AE40	I/O	Suspend	Native	U_USB_OC_R_#0	--	8.2k pull-up to +3V_S5	Native
GPIO[60]	SML0ALERT#/GPIO60	AG35	I/O	Suspend	Native	S_SMI0LALERT#	--	10k pull-up to +3V_S5	NU
GPIO[61]	SUS_STAT#/GPIO61	AD37	I/O	Suspend	Native	S_SUS_STAT#	--	10k pull-up to +3V_S5 (dummy	NU
GPIO[62]	SUSCLK/GPIO62	W36	I/O	Suspend	Native	S_SUSCLK_R	PU	--	Native
GPIO[63]	SLP_S5#/GPIO63	AA35	I/O	Suspend	Native	S_SLP_S5#	--	--	Native
GPIO[64]	CLKOUTFLEX0/GPIO64	AV8	I/O	Core	Native	S_TP_CLKOUTFLEX0	20K IN-PD	---	NU
GPIO[65]	CLKOUTFLEX1/GPIO65	AT9	I/O	Core	Native	C_14M_SIO_R	20K IN-PD	---	Native
GPIO[66]	CLKOUTFLEX2/GPIO66	AV9	I/O	Core	Native	S_TP_CLKOUTFLEX2	20K IN-PD	---	NU
GPIO[67]	CLKOUTFLEX3/GPIO67	AU8	I/O	Core	Native	C_14M_TPM_R	20K IN-PD	---	Native
GPIO[68]	TACH4/GPIO68	AT30	I/O	Core	GPI	S_GPI_BRD_REV2	20K IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	I
GPIO[69]	TACH5/GPIO69	AV35	I/O	Core	GPI	S_USB_HDR_DET#	20K IN-PU (only on TACH5)	8.2k pull-up to +3V	I
GPIO[70]	TACH6/GPIO70	AK28	I/O	Core	Native	S_GPIO70	20K IN-PU (only on TACH6)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[71]	TACH7/GPIO71	AT34	I/O	Core	Native	S_GPIO71	20K IN-PU (only on TACH7)	10k pull-up to +3V 10k pull-down to GND (dummy)	Strapping
GPIO[72]	GPIO72	AJ40	I/O	Suspend	Native (Mobile Only)	S_GPIO72		10k pull-up to +3V_S5	NU
GPIO[73]	PCIECLKRQ0#/GPIO73	W34	I/O	Suspend	Native	S_FP_CHAS_DET#		10k pull-up to +3V_S5	NU
GPIO[74]	SML1ALERT#/TEMP_ALERT#/ GPIO74 PCHHOT#	AJ39	I/O	Suspend	Native	TMIN_SHIFT	--	8.2k pull-up to +3V_S5 330k pull-down to GND (Dummy)	O
GPIO[75]	SML1DATA/GP75	AK33	I/O	Suspend	Native	S_SML1DATA	PU	2.2k pull-up to +3V_S5	Native

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Title: **GPIO Table**

DWG NO: *D7 Micro* | Rev: X01

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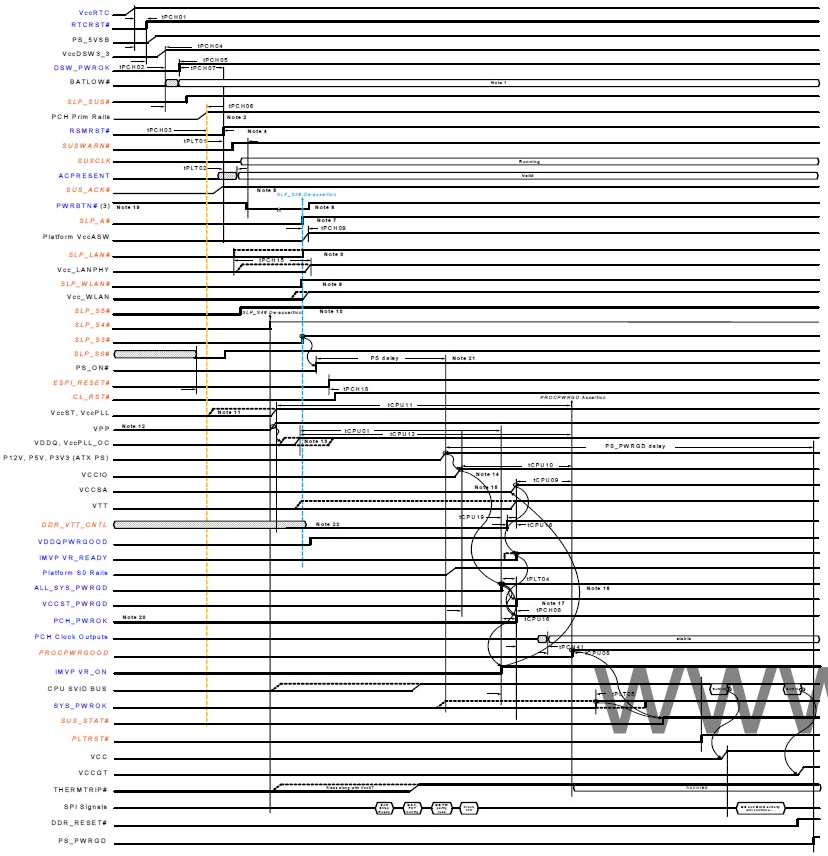
POWER ON Timing Diagram



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Title: **Power On Sequence**

DWG NO: *D7 Micro*

Rev: X01

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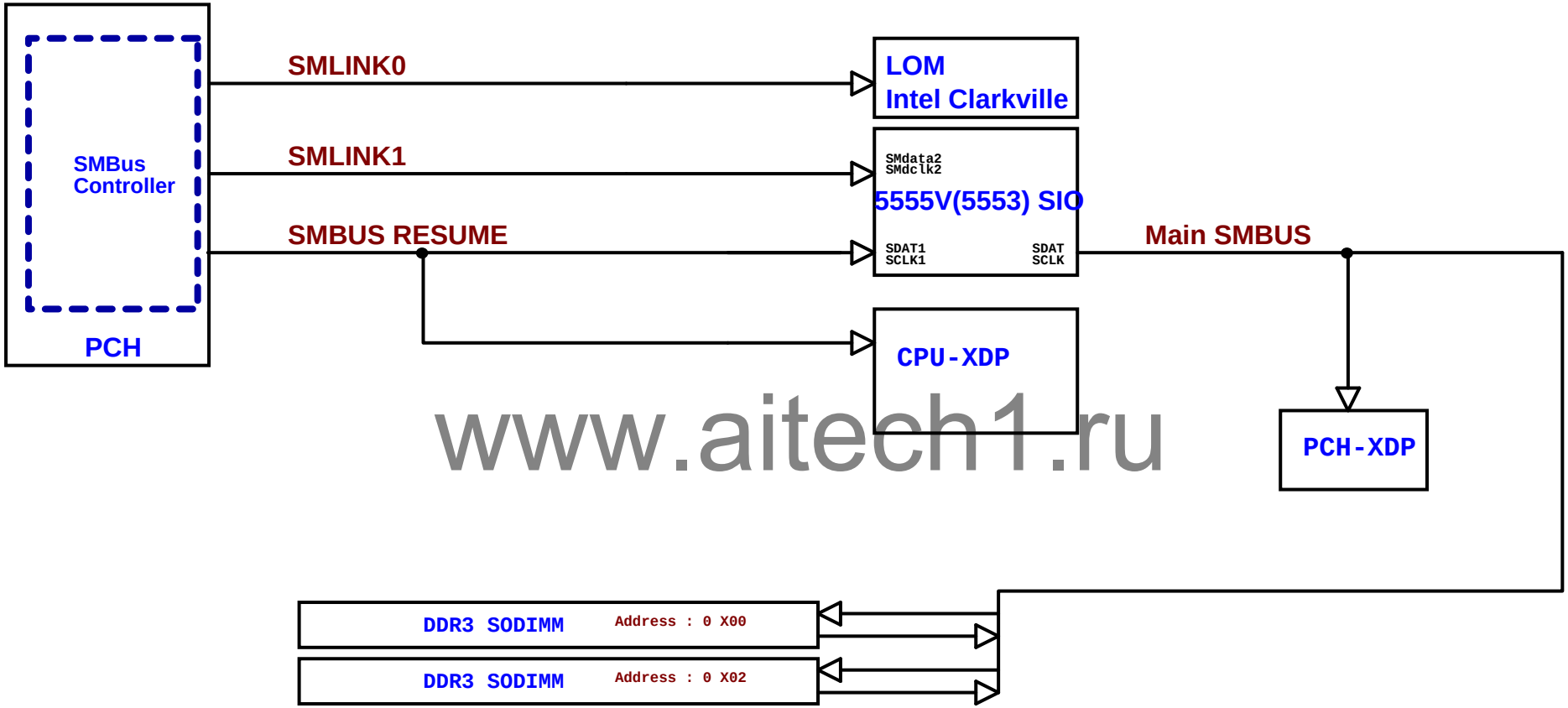
SMBUS DIAGRAM



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Title: BLOCK DIAGRAM

DWG NO: D7 Micro

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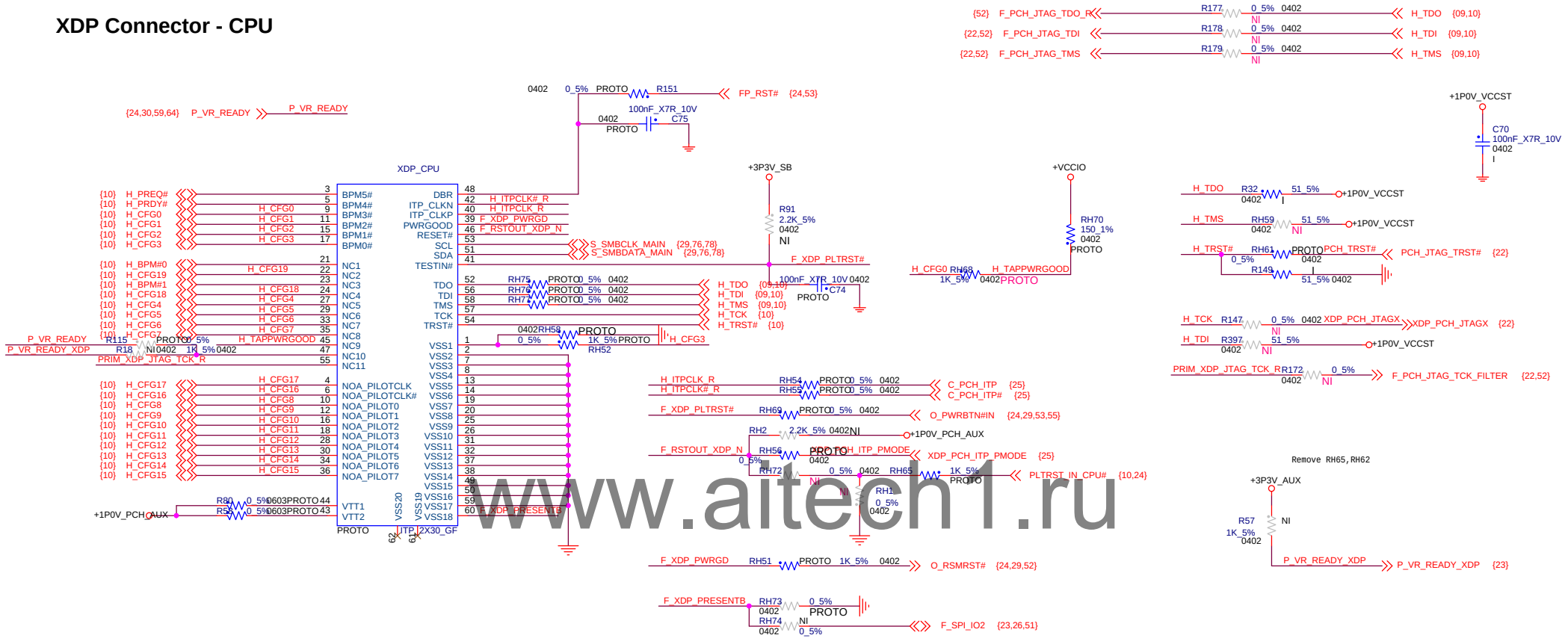
XDP Connector - CPU



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Title

XDP

DWG NO

D7 Micro

Rev **X01**

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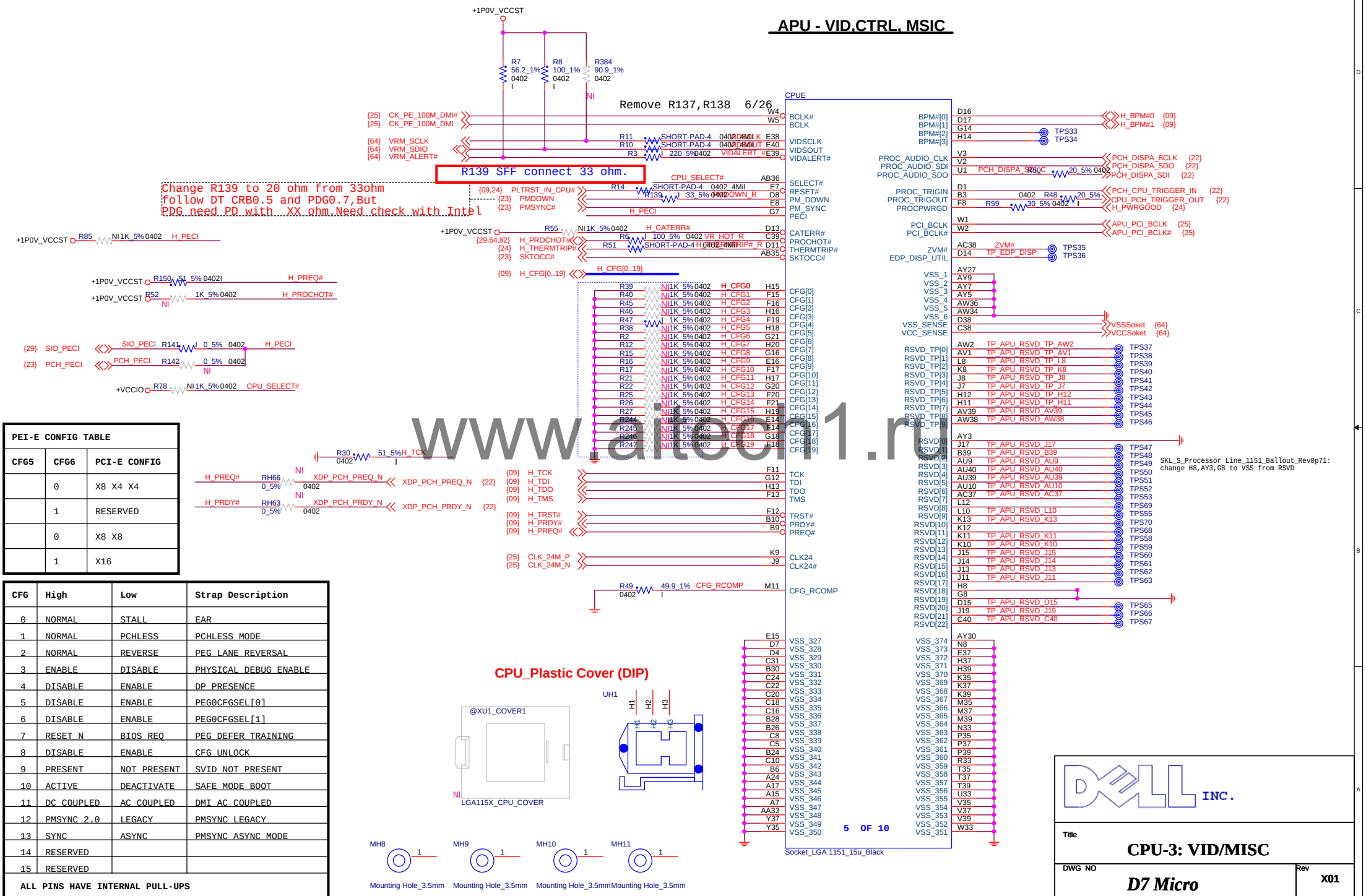
APU - VID,CTRL, MSIC



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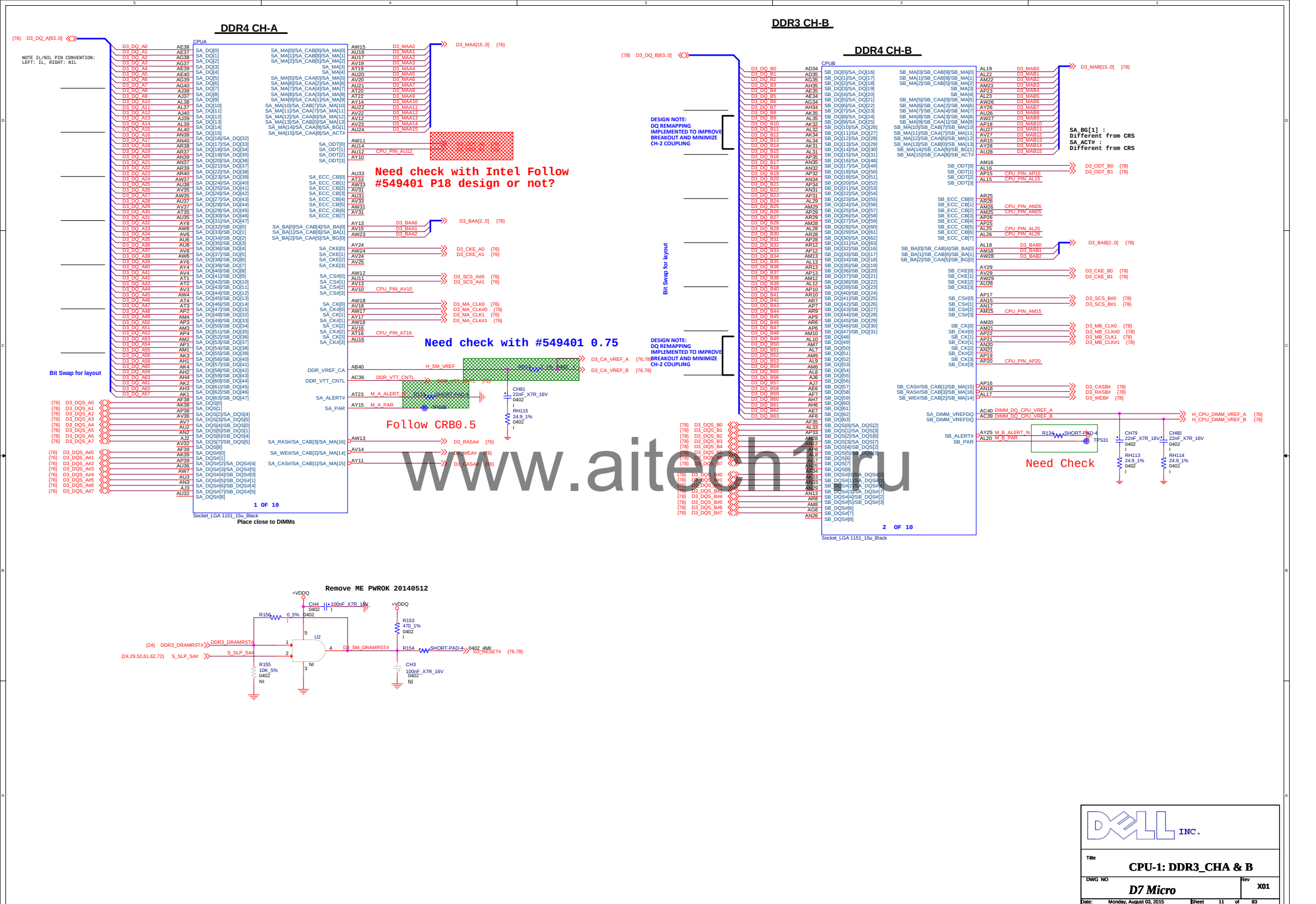
PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
	0	X8 X4 X4
	1	RESERVED
	0	X8 X8
	1	X16

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG LANE REVERSAL
3	ENABLE	DISABLE	PHYSICAL DEBUG ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8	DISABLE	ENABLE	CFG UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI AC COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYNC	PMSYNC ASYNC MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS


DDR4 CH-A
DDR3 CH-B
DDR4 CH-B
CPUA
CPUB
NOTE IL/NIL PIN CONVENTION:
LEFT: IL, RIGHT: NIL
Need check with Intel Follow #549401 P18 design or not?
Need check with #549401 0.75
Follow CRB0.5
Need Check
Bit Swap for layout
DESIGN NOTE: DQ REMAPPING IMPLEMENTED TO IMPROVE BREAKOUT AND MINIMIZE CH-2 COUPLING
SA_BG[1] : Different from CRS
SA_ACT# : Different from CRS
1 OF 10
2 OF 10
Socket_LGA 1151_15u_Black
Place close to DIMMs
Remove ME PWROK 20140512
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Title
CPU-1: DDR3_CHA & B
DWG NO
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CPU-1: DDR3_CHA & B

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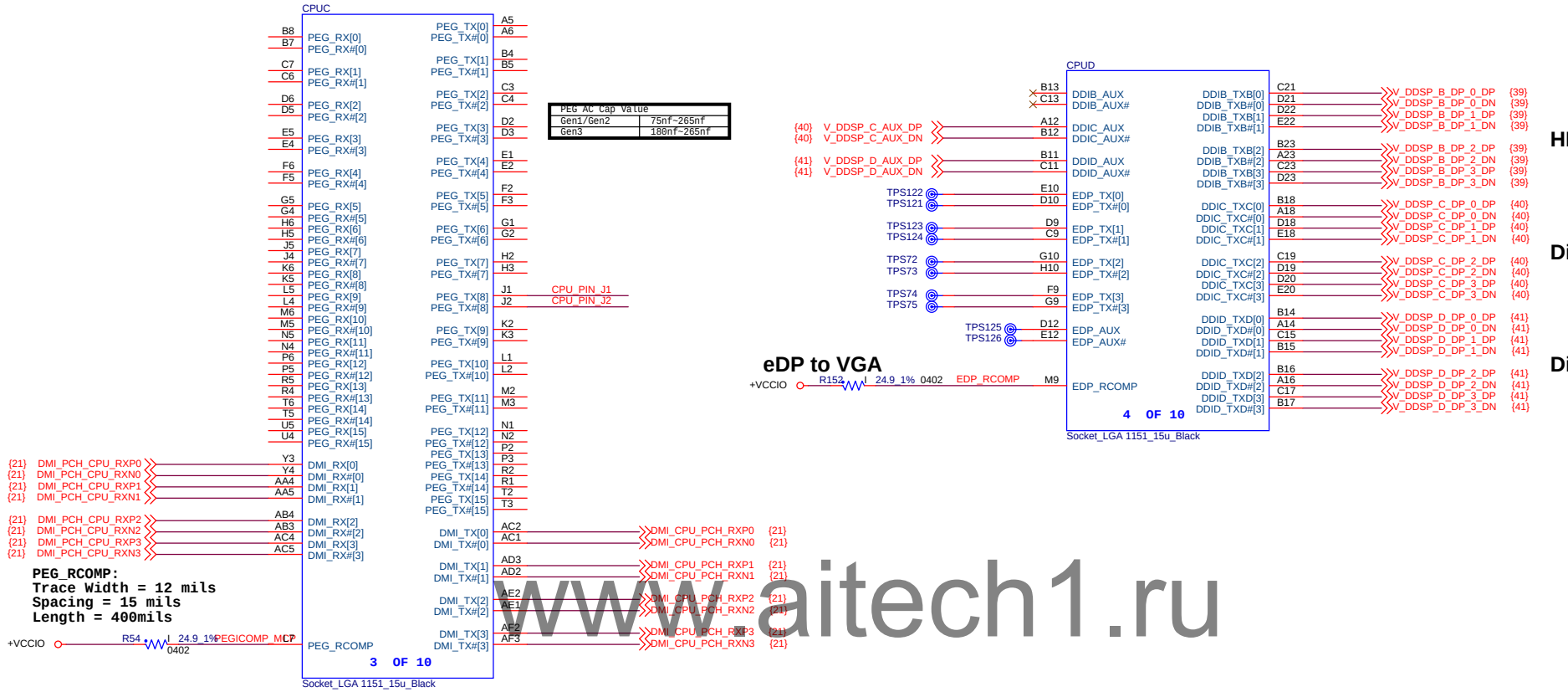
MCP - PCIE,DMI,FDI,DDI



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CPU-4: FDI/PCIe/DMI/DP

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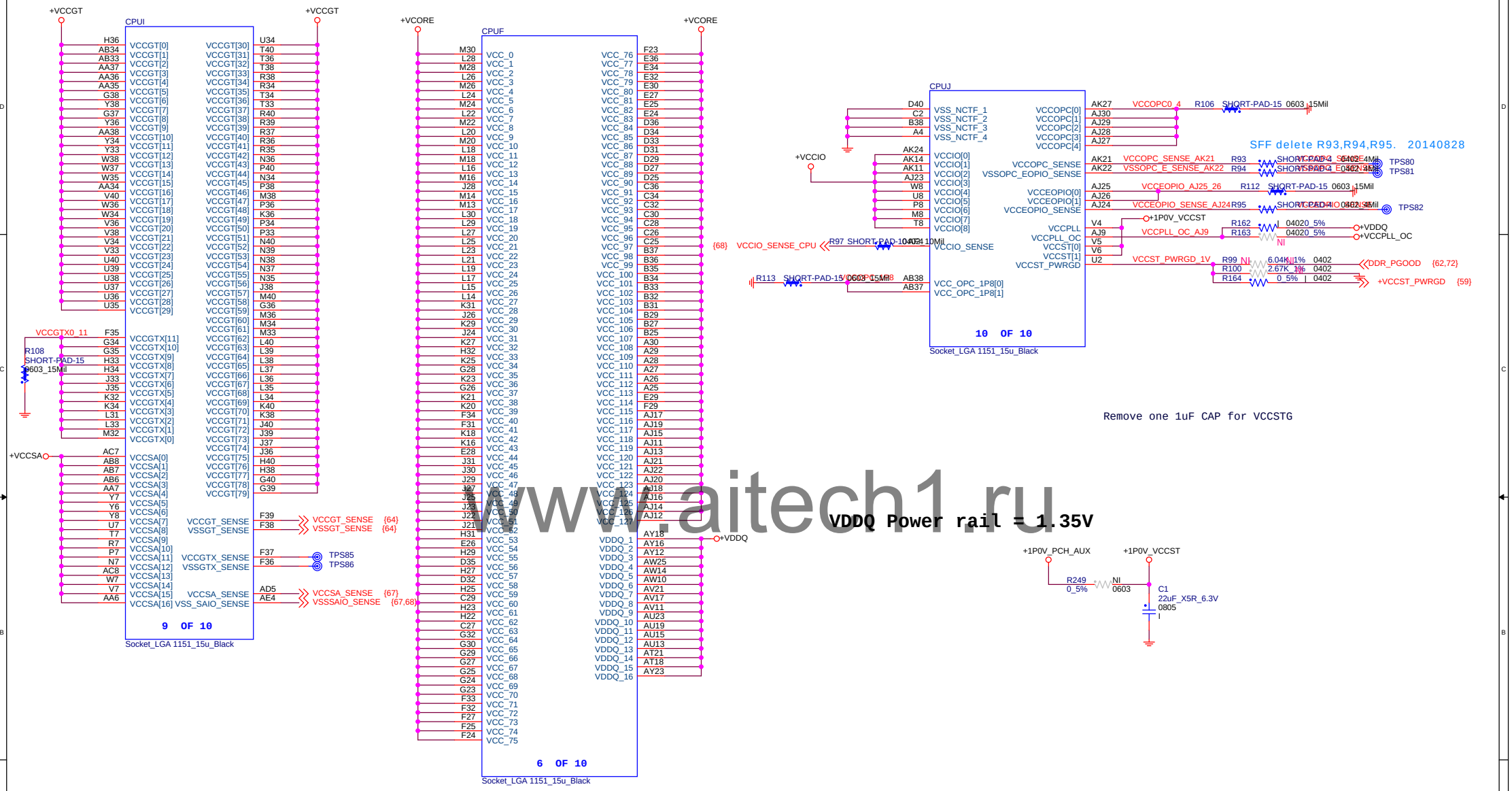

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CPU-5: Vcore

DWG NO *D7 Micro* Rev X01

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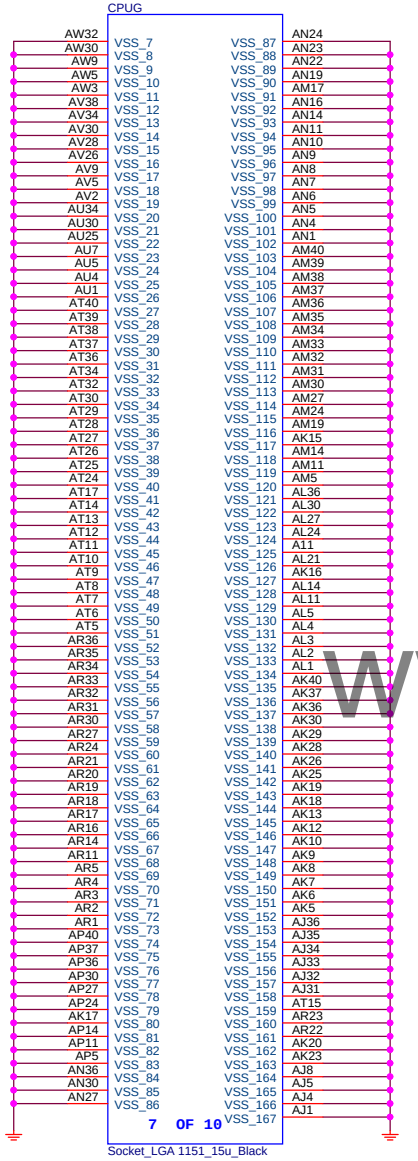

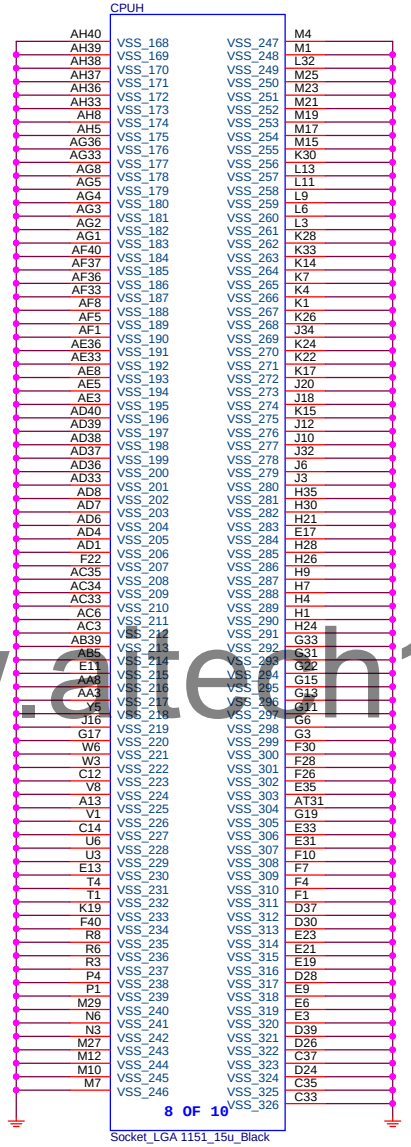

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CPU-6: GND

DWG NO

D7 Micro

Rev X01

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STRAPPING Table

PCH side

Table 36-18. Strapping Signals (Sheet 1 of 2)

Name	Type	Recommendations	Reason/Impact
SPKR	I	**Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2k-10k Ohm weak pull-up resistor.	
INIT3_3V#	I	Do not pull low.	
GPIO55	I/O	**Default Mode:** Internal pull-up. **Top Block Swap Mode:** Connect to ground with 4.7k Ohm weak pull-down resistor.	
SATA1GP/ GPIO19, GPIO51	I/O	**Default (SPI)** Left both SATA1GP/GPIO19 and GPIO51 floating. No pull up required. **Boot from PCI** Connect SATA1GP/GPIO19 to ground with 1k Ohm pull-down resistor. Leave GPIO51 Floating. **Boot from LPC** Connect both SATA1GP/GPIO19 and GPIO51 to ground with 1k Ohm pull-down resistor.	If LPC is selected BIOS may still be placed on LPC, but all platforms with PCH require SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. Booting to PCI is intended for debut/testing only. Boot BIOS Destination Select to LPC/PCI by functional strap or via Boot BIOS Destination Bit will not affect SPI accesses initiated by Management Engine or Integrated GbE LAN.
GPIO53	I/O	Do not pull low. Connect to ground with 1k Ohm pull-down resistor.	ESI strap for server platform ONLY
HDA_SDO	I/O	**Default** Do not pull high. **Disable ME in Manufacturing Mode** Connect to VccSusHDA with 1k Ohm pull-up resistor through a jumper.	Flash descriptor Override
SPI_MOSI	I/O	Internal weak pull down.Do not pull high.	DMI RX Termination Voltage
SAAT3GP/ GPIO37	I/O	**Enable TLS:** Pull up with 1k Ohm to VccSus3.3. **Default (Disable TLS):** Leave NC. Internal pull down.	TLS confidentiality
GPIO8	I/O	Internal weak pull up.Do not pull low.	

Table 36-18. Strapping Signals (Sheet 2 of 2)

Name	Type	Recommendations	Reason/Impact
GPIO62/ SUSCLK	I/O	Internal weak pull up. Do not pull low.	On die PLL voltage regulator
GPIO36	I/O	Internal weak pull down. Do not pull high.	
DDPB_CTRL _DATA DDPC_CTRL _DATA DDPD_CTRL _DATA		Straps for digital ports B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K ohms resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2k ohms resistor. This signal should always be routed longer than SDVO/ DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage to the display connector. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2k ohmsresistor. This signal should always be routed longer than SDVO/DDPC_CTRLCLK by an inch.	

CPU side

Signal Name	Description	Direction/ Buffer Type
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. • **CFG[1:0]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed. • **CFG[3]:** PCI Express* Static x4 Lane Numbering Reversal. – x1 = Normal operation – x0 = Lane numbers reversed • **CFG[4]:** Reserved configuration lane. A test point may be placed on the board for this lane. • **CFG[6:5]: PCI Express* Bifurcation:** [1] – x00 = 1 x8, 2 x4 PCI Express* – x01 = reserved – x10 = 2 x8 PCI Express* – x11 = 1 x16 PCI Express* • **CFG[19:7]:** Reserved configuration lanes. A test point may be placed on the board for these lands.	I CMOS

Strapping Options Flash

GNT1#	SATA1GP/GPIO19	Routing
0	0	Flash Cycles Routed to LPC
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to SPI

Table 34-6. PCH Digital Display Strapping Signals

Checklist Item	Recommendations	Direction	Comments
DDPC_CTRLDATA	Straps for digital port B, C and D. For DisplayPort* - Should be pulled to 3.3V through a 2.2K W resistor to configure digital port. For DVI/HDMI configuration, the signal should be routed through the level shifter to the display connector. The signal is pulled to 3V before the level shifter and 5V before the display connector through a 2.2KW resistor. This signal should always be routed longer than DDPC_CTRLCLK by an inch. For DVI/HDMI configuration with the Cost Reduced level shifter, the signal should be routed through the pass gate sourced from 3.3V voltage. The signal is pulled to 3V before the pass gate and 5V before the display connector through a 2.2KW resistor and a Schottky diode. This signal should always be routed longer than DDPC_CTRLCLK by an inch. Also ensure schottky diode is not shared with DDPC_CTRLCLK.	BI	

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SIO SMSC5555

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT

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Title

GPIO/IRQ/IDSEL Table

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Title

CPU-1: DDR3_CHA & B

DWG NO

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Rev

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Rev

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Rev

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DWG NO

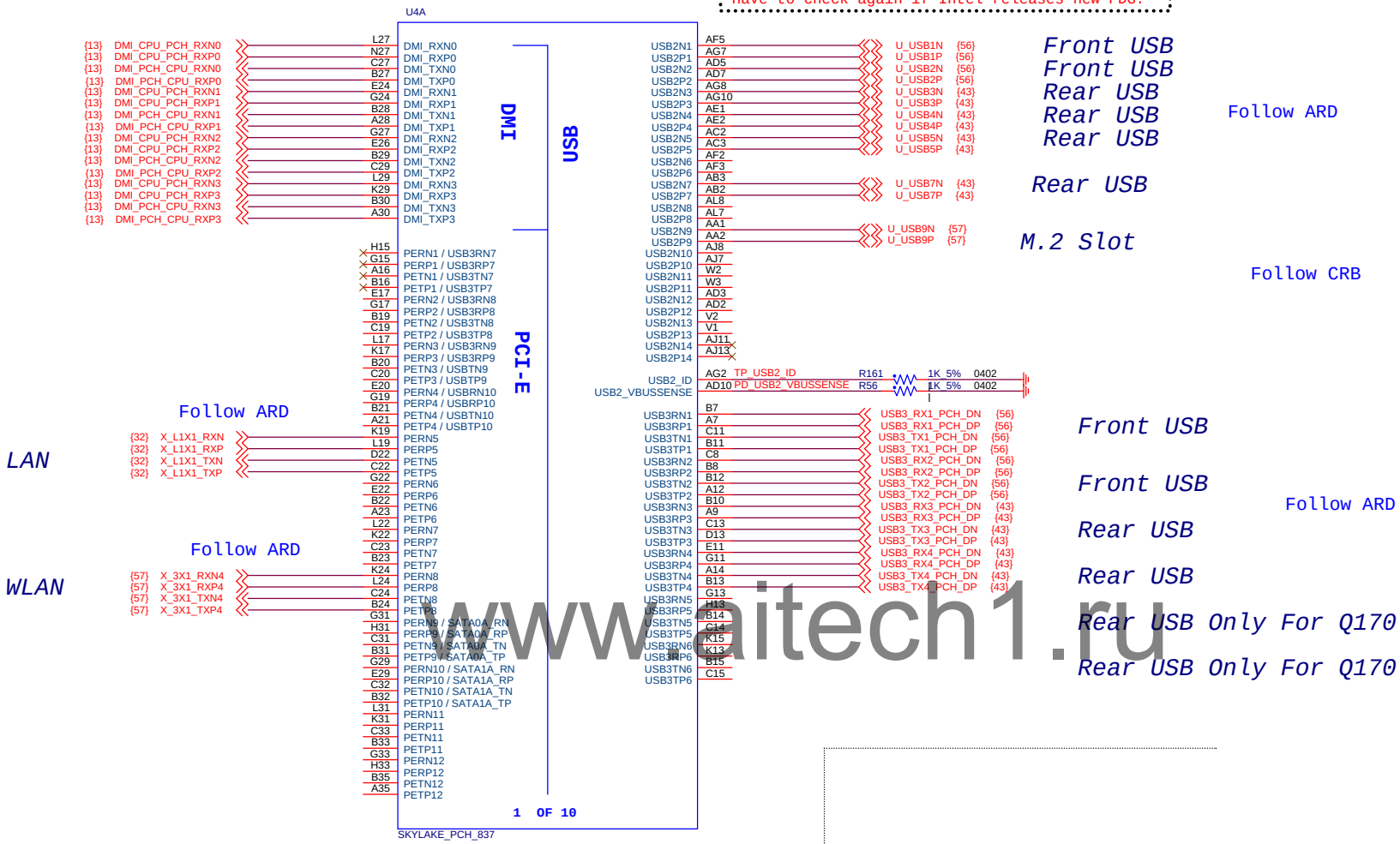
D7 Micro

Rev

X01

Date: Monday, August 03, 2015

USB3 and USB2 port mapping is not clear in PDG.
Have to check again if Intel releases new PDG.



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Have to check the flexible IO definition.

Refer to PDG P169
Gigabit LAN support is available on HSIO ports 10, 11, 15, 18.

Refer to PDG P169
PCIe ports 1, 5, 9, 13, 17 can support up to x4 lanes with the following possible lane configuration
1x4, 2x2, 1x2, + 2x1, and 4x1

PCA spec require
J31 = x1 slot
J32 = x1 slot
J42 = x16 slot (x4signal)

PCH PCIe/USB2/USB3/SATA Routing
Breakout
MS : 8/3.5/4/3.5/4 (Group)
MS : 15/3.5/4/3.5/15 (Other)

Main
MS : 12/4/4/4/12 (Group)
MS : 15/4/4/415 (Other)

PS: 20mils spacing for Tx to Rx or Rx to High Speed clock

TBD

USB 2/3 port MAP and OC

	USB3	USB2	OC
EVT	NI	NI	NI
DVT	I	I	NI
PVT1	NI	NI	I
PVT2+	I	I	NI
MVB,A	NI	NI	I
1st major ECN	I	I	NI
2nd major ECN	NI	NI	I
3rd major ECN	I	I	NI
3rd major ECN			
EVT	NI	NI	I
DVT	I	I	NI
PVT1	NI	NI	I
PVT2+	I	I	NI
MVB,A	NI	NI	I
1st major ECN	I	I	NI
2nd major ECN	NI	NI	I
3rd major ECN	I	I	NI

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Title
PCH-1: DMI/USB/PCIe

DWG NO
D7 Micro

Rev
X01

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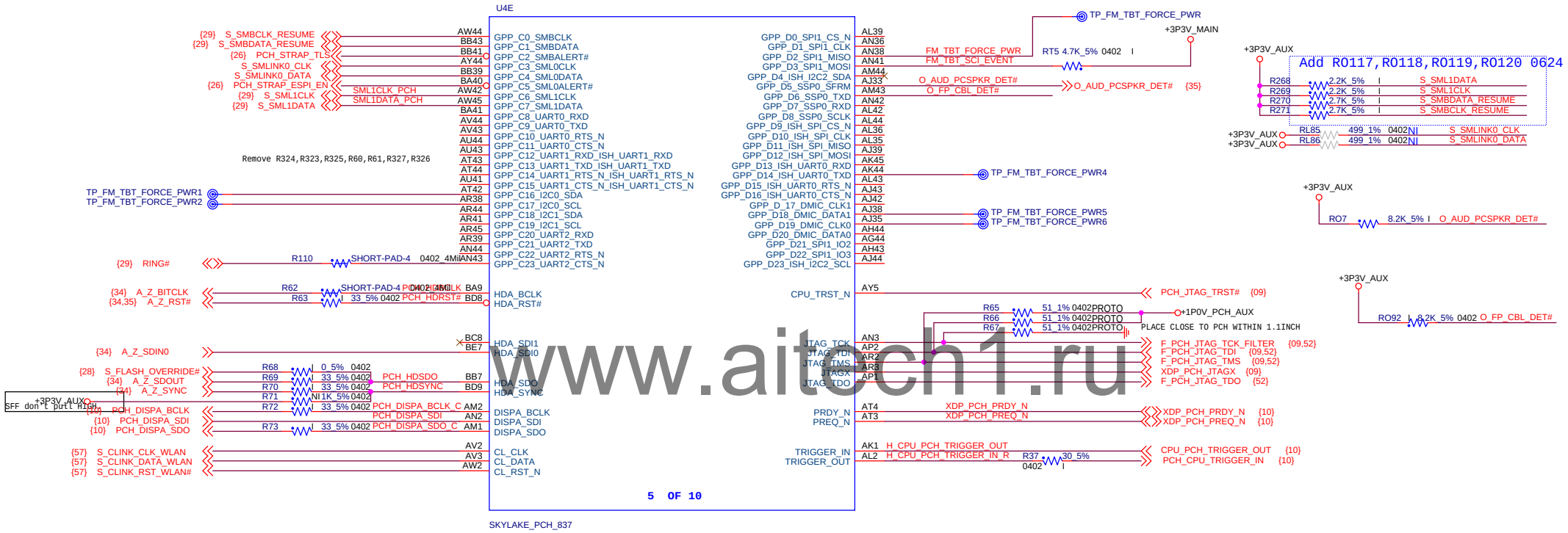

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Title: PCH-3:SPI/HDA/ACPI/MISC

DWG NO: D7 Micro

Rev: X01

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Title: PCH-2: SATA/HOST/GPIO

DWG NO: D7 Micro

Rev: X01

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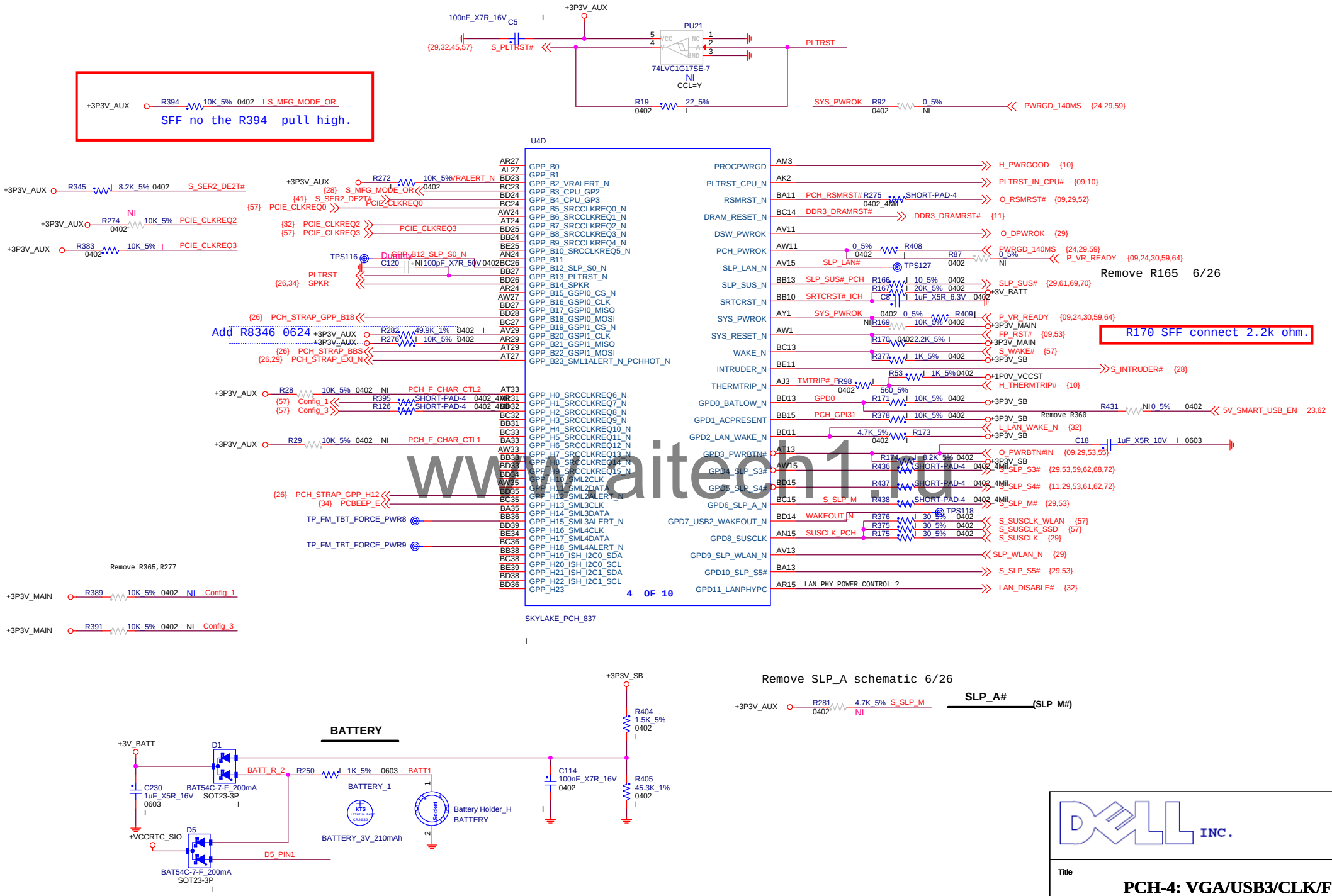

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Title

PCH-4: VGA/USB3/CLK/FDI

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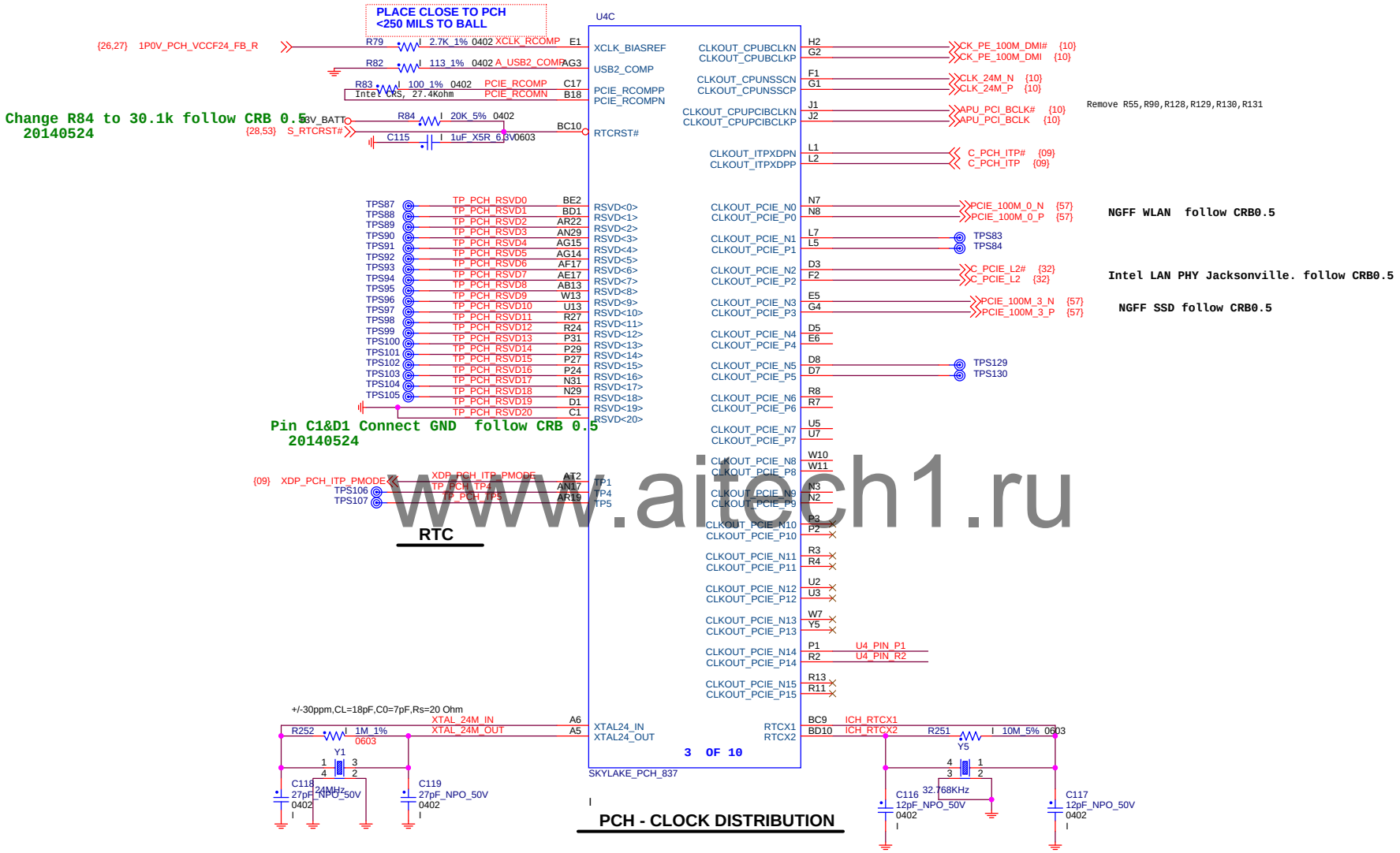

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Title

PCH

DWG NO

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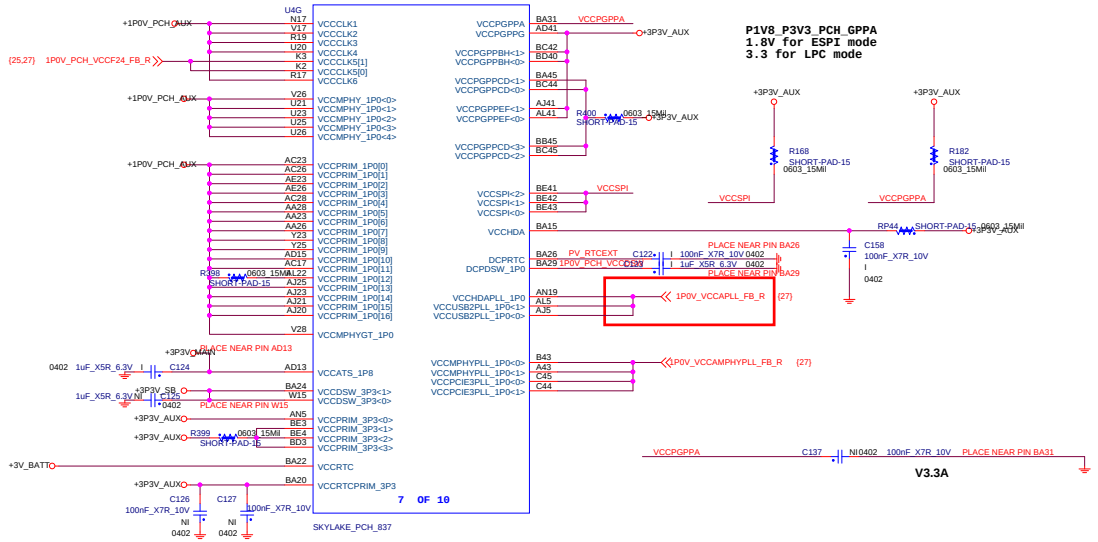

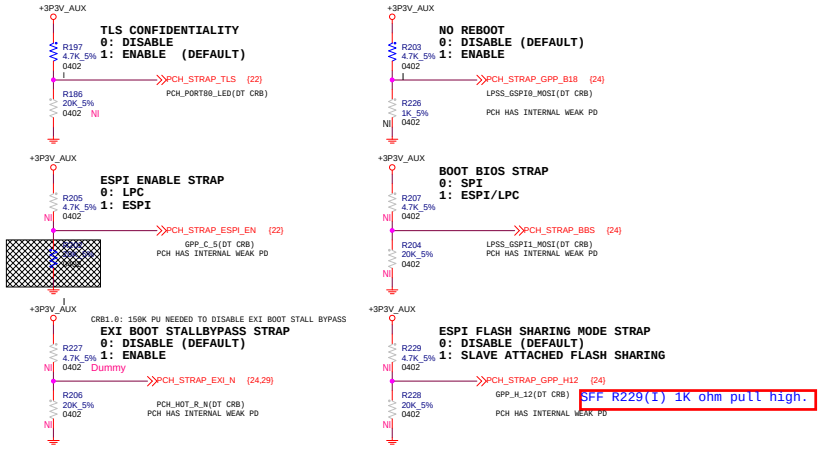

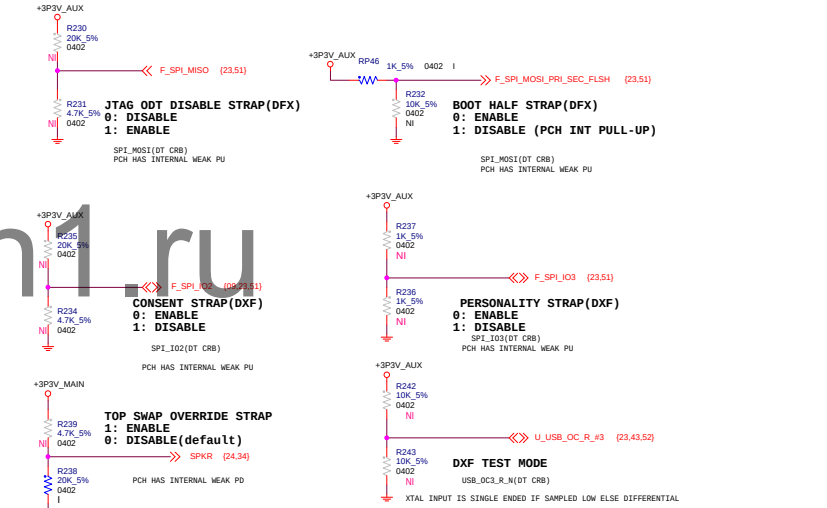

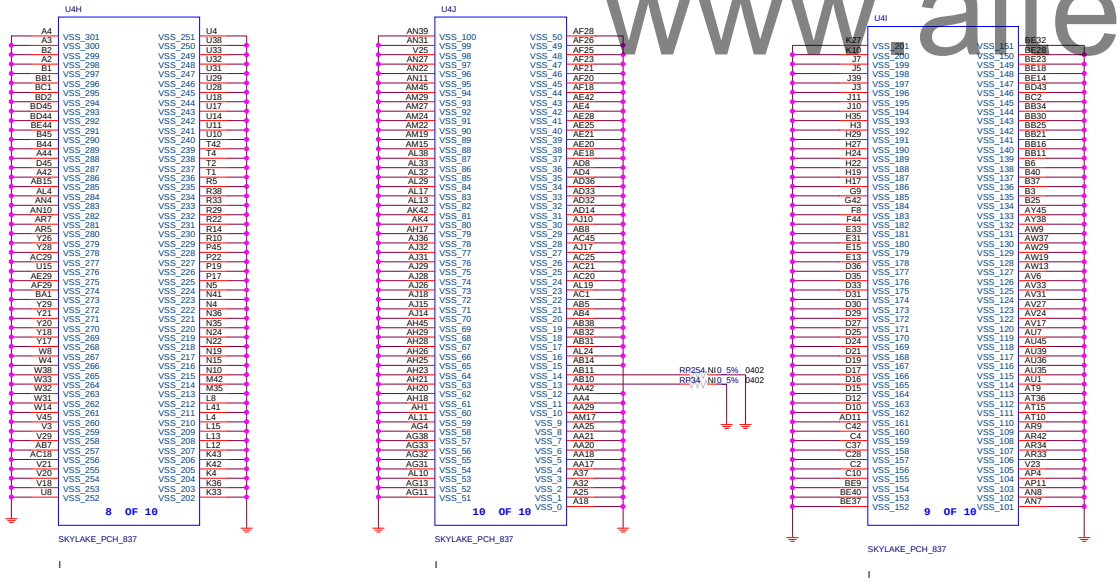

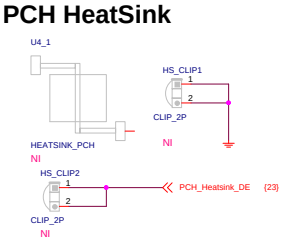

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Title: **PCH-5: POWER**

DWG NO: *D7 Micro*

Rev: X01

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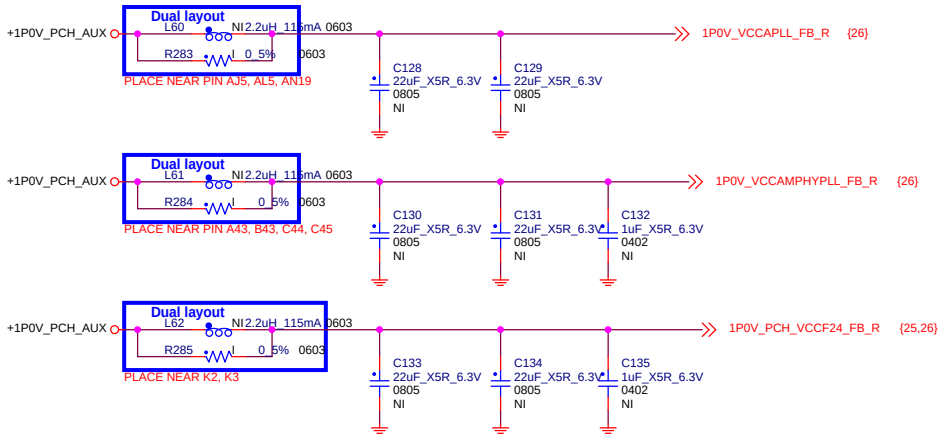
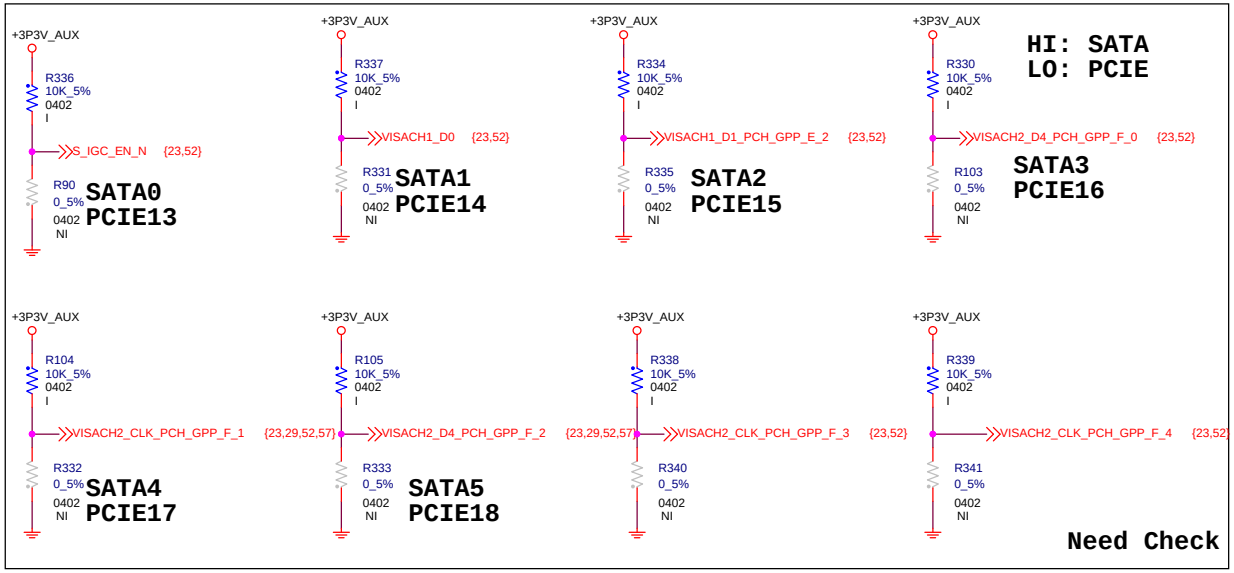
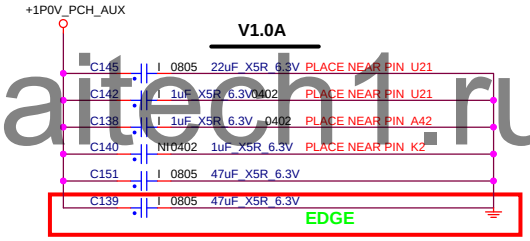
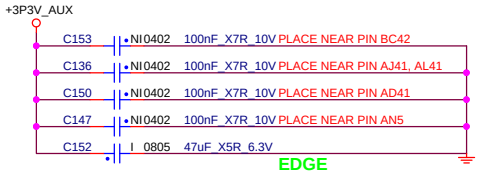
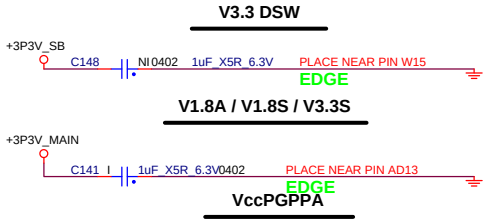
SKYLAKE Decoupling & filter

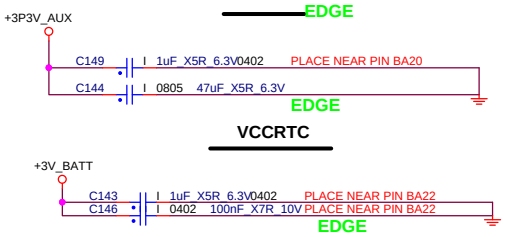












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Power Plane Isolation

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

DELL INC.

Title

PCH-9: STRAP OPTION

DWG NO *D7 Micro* Rev X01

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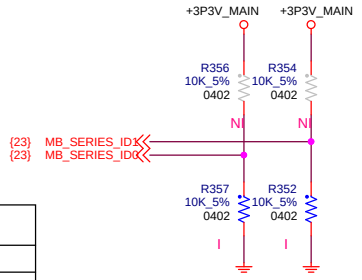
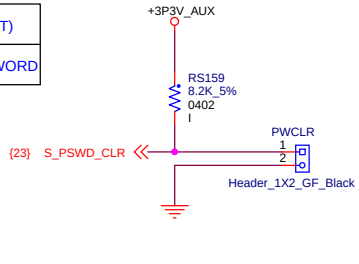
SKU ID



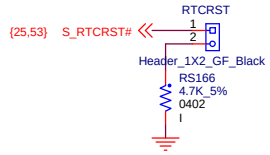
ID1	ID0	Type
0	0	3
0	1	5
1	0	7
1	1	Farallon

Clear Password

PSWD	1-2: NORMAL(DEFAULT)
	EMPTY: CLEAR PASSWORD

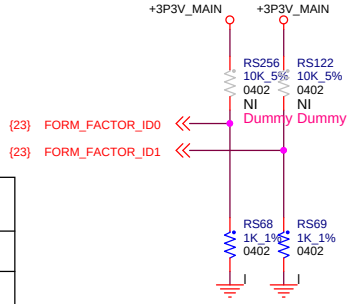


CLR_CMOS



RTCRST	1-2: CLR CMOS
	EMPTY(Default)

Chassis ID



ID1	ID0	Type
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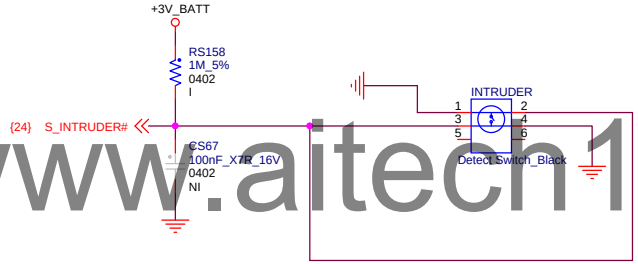
1	0	CT
0	1	SFF
0	0	Micro

Chassis Intruder

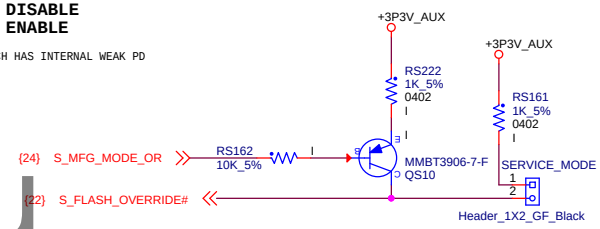


Servece Mode

ME Disable (Flash overide)

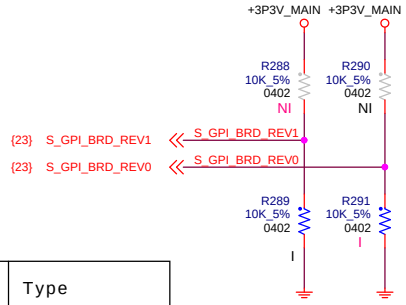
FLASH DESCRIPOR SECURITY OVERRIDE
0: DISABLE
1: ENABLE

PCH HAS INTERNAL WEAK PD



SERVICE_MODE	1-2: ME DISABLE
	EMPTY: NORMAL(DEFAULT)

BOARD ID



ID1	ID0	Type
1	1	X02
1	0	X01
0	1	X00
0	0	B00/A00

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DELL INC.

Title
PCH-8: MISC CONN/BEEP/ID

DWG NO
D7 Micro

Rev
X01

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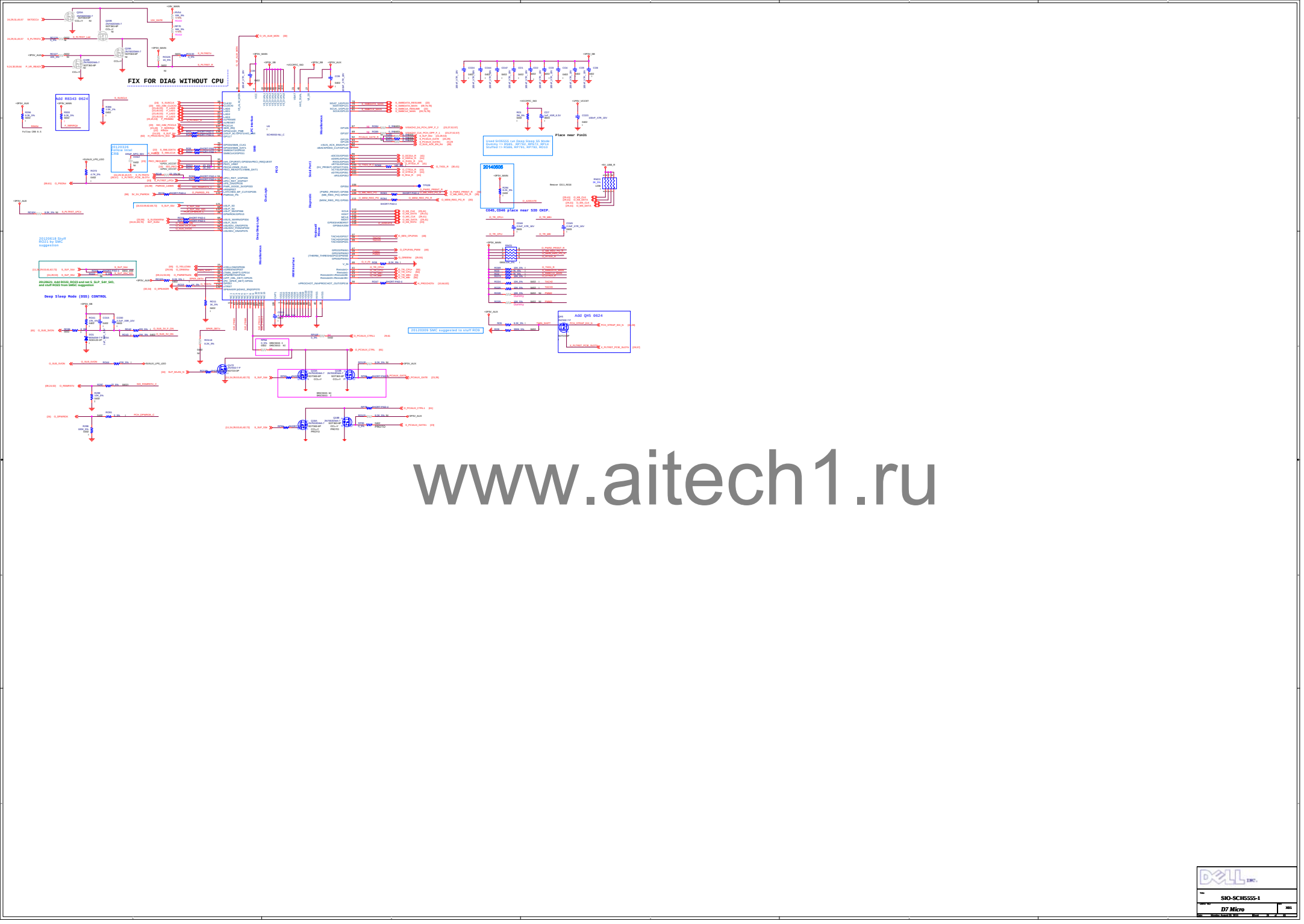

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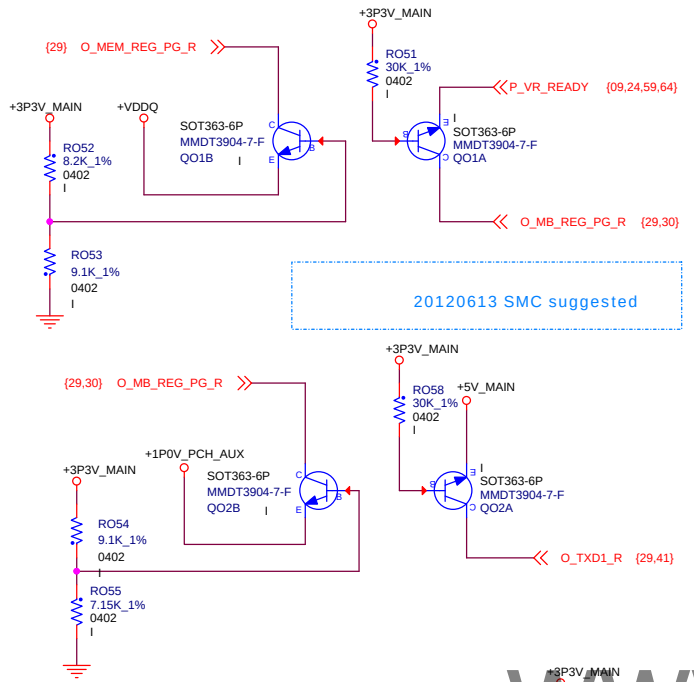
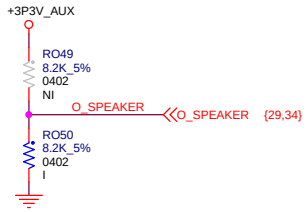
5555 PRE-POST DIAG Monitor



SIO STRAPING



SIO STRAPING

	SPEAKER	
	Diag_En	
PULL HIGH	Disable	
PULL LOW	Enable	

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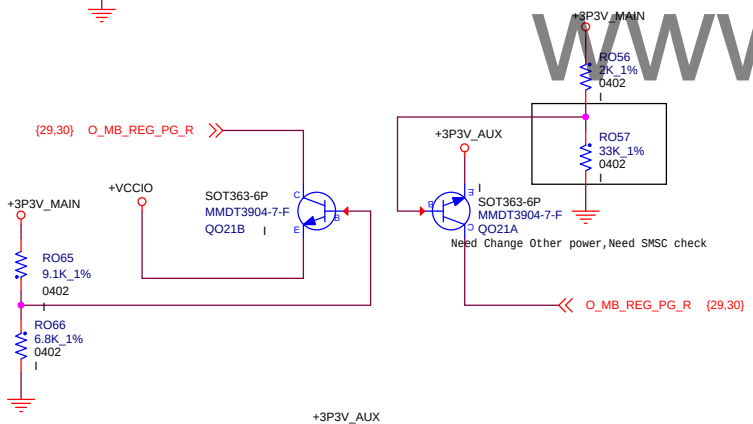
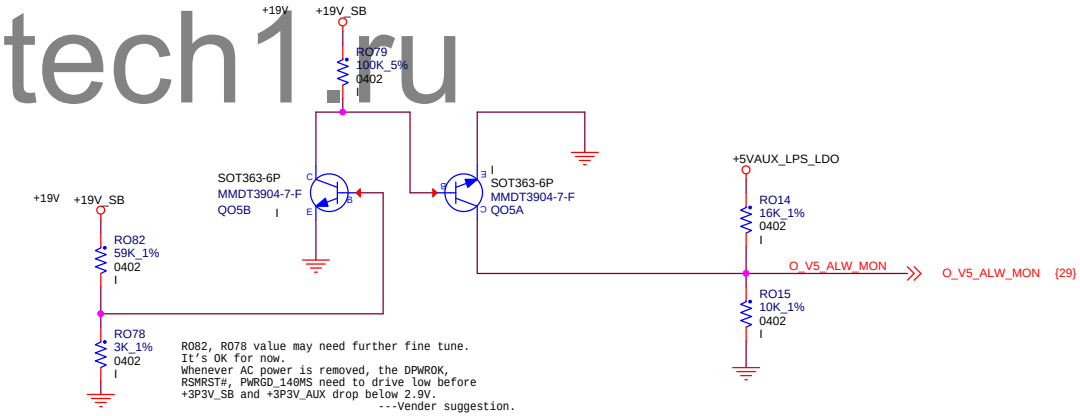
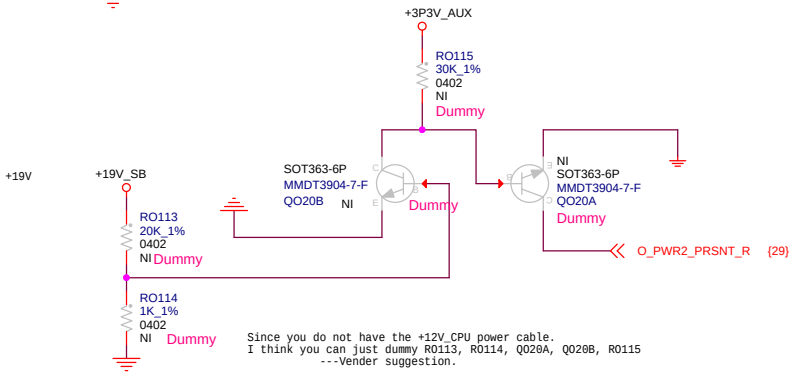


SIO5555 V5_ALW Monitor





DELL INC.

Title

SIO-SCH5555-2

DWG NO

D7 Micro

Rev

X01

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DELL INC.

Title

LAN:Intel Clarkville

DWG NO

D7 Micro

Rev

X01

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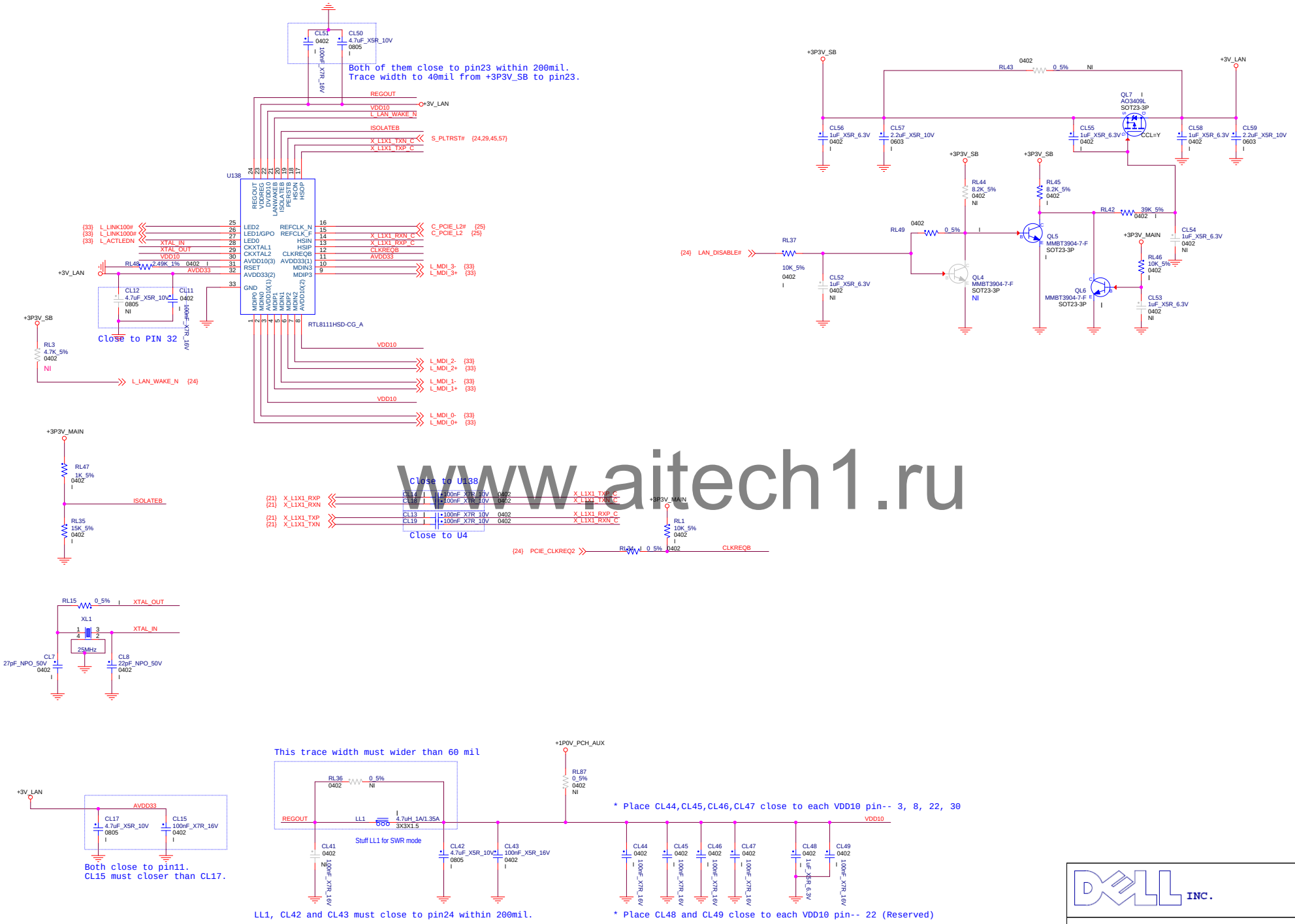

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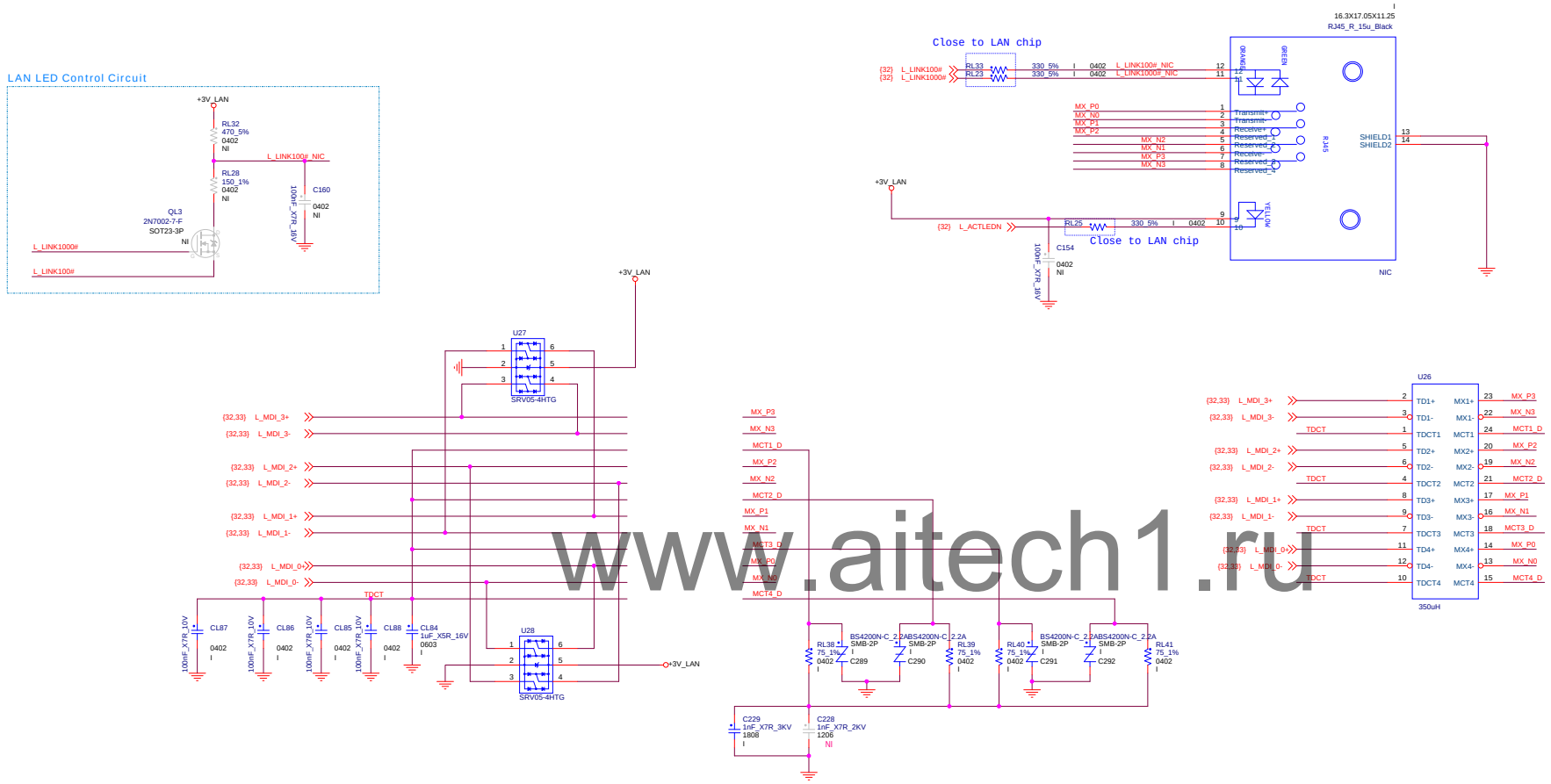
LAN CONNECTOR



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LAN POWER

DELL INC.

Title: LAN Power & LAN/USB Conn

DWG NO: D7 Micro

Rev: X01

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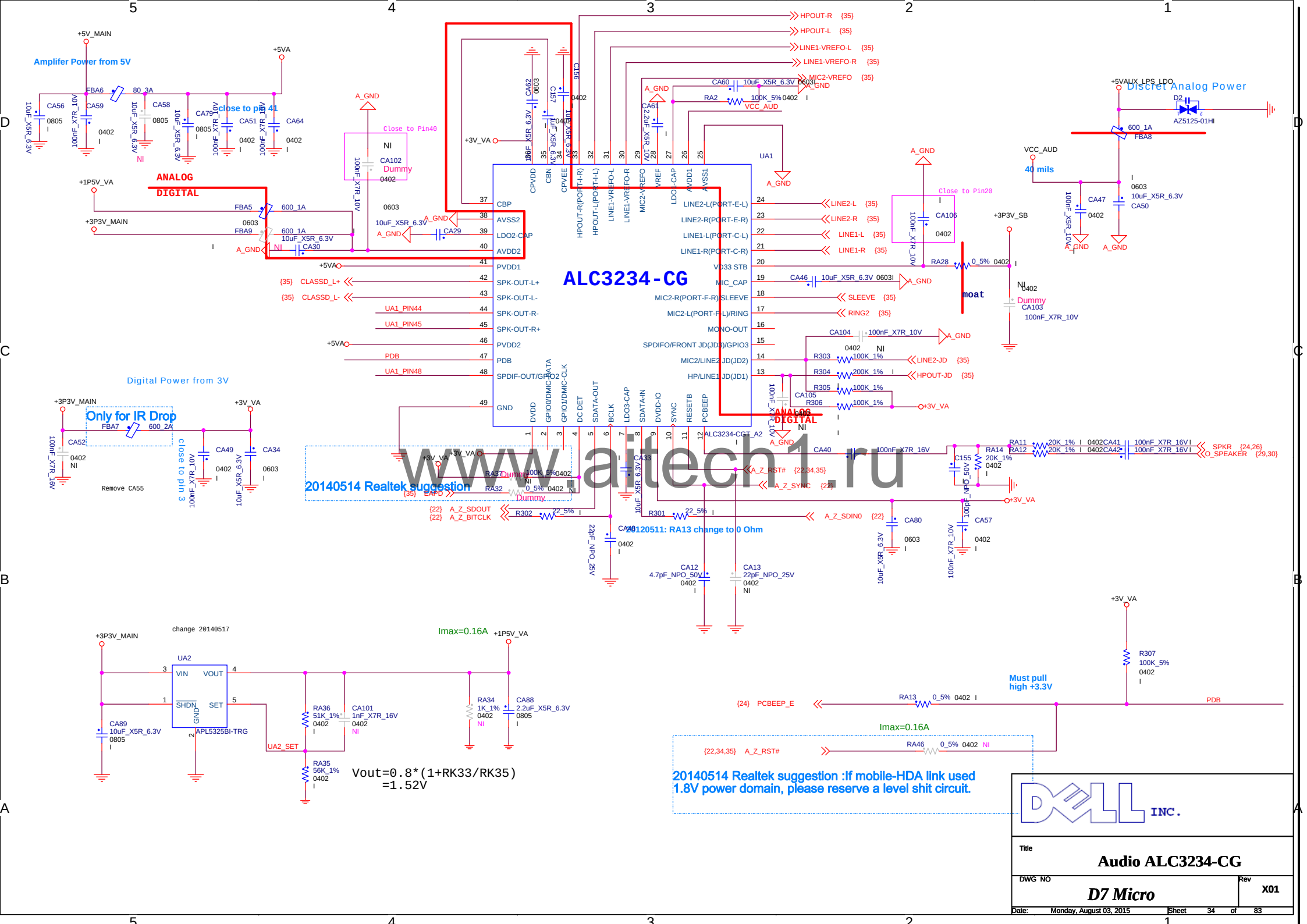
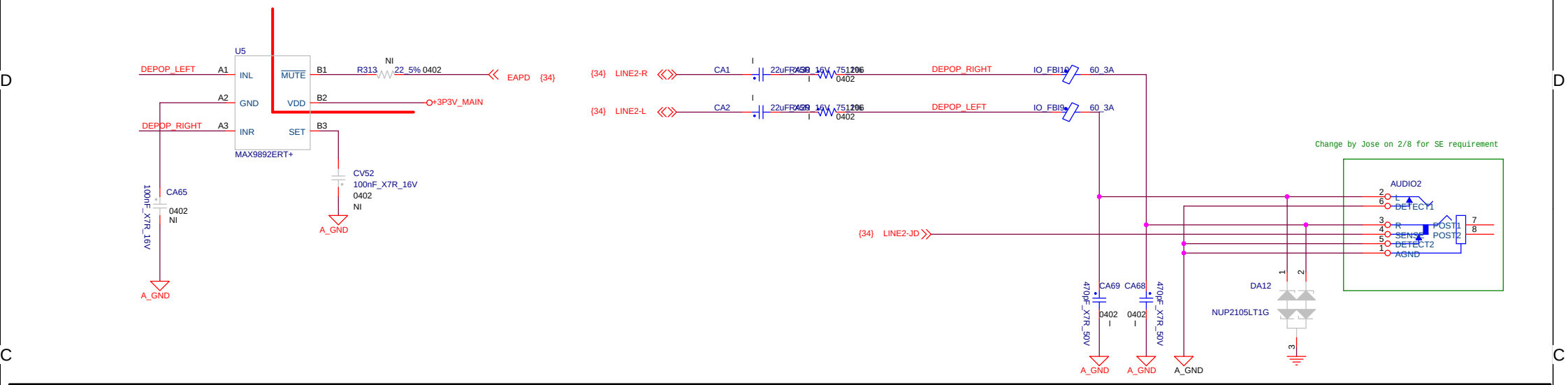
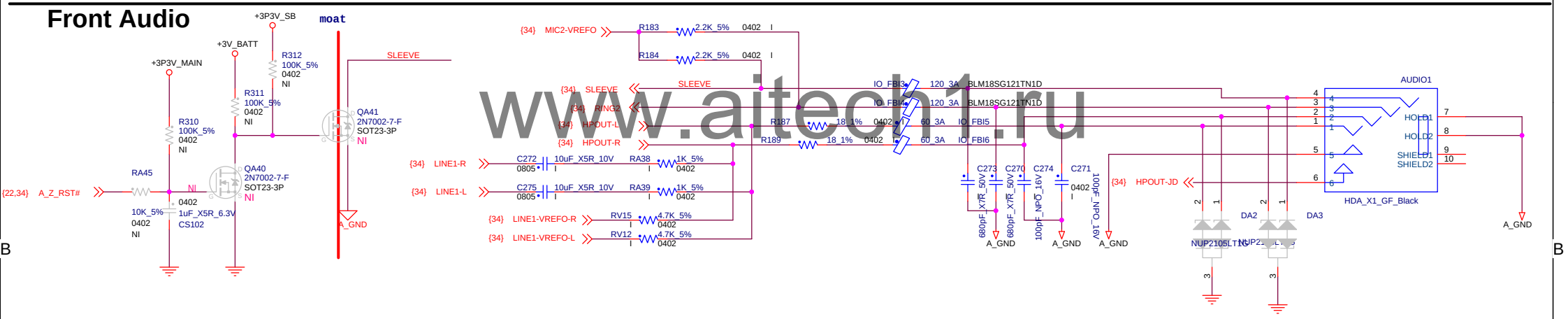


www.aitech1.ru

Front Audio Jack



Front Audio



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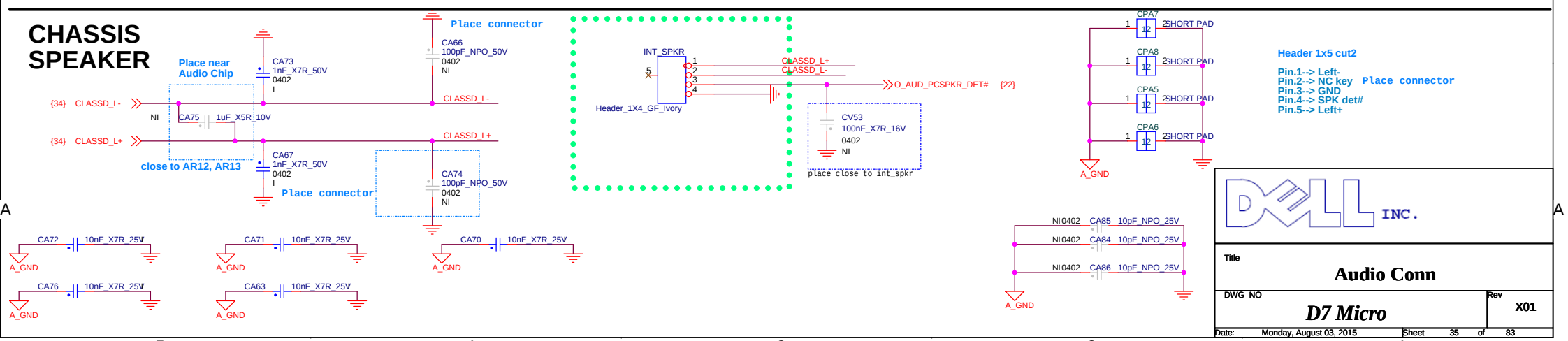
CHASSIS SPEAKER



DELL INC.

Title: **Audio Conn**

DWG NO: *D7 Micro*

Rev: X01

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DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015

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DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015

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DELL INC.

Title

CPU-1: DDR3_CHA & B

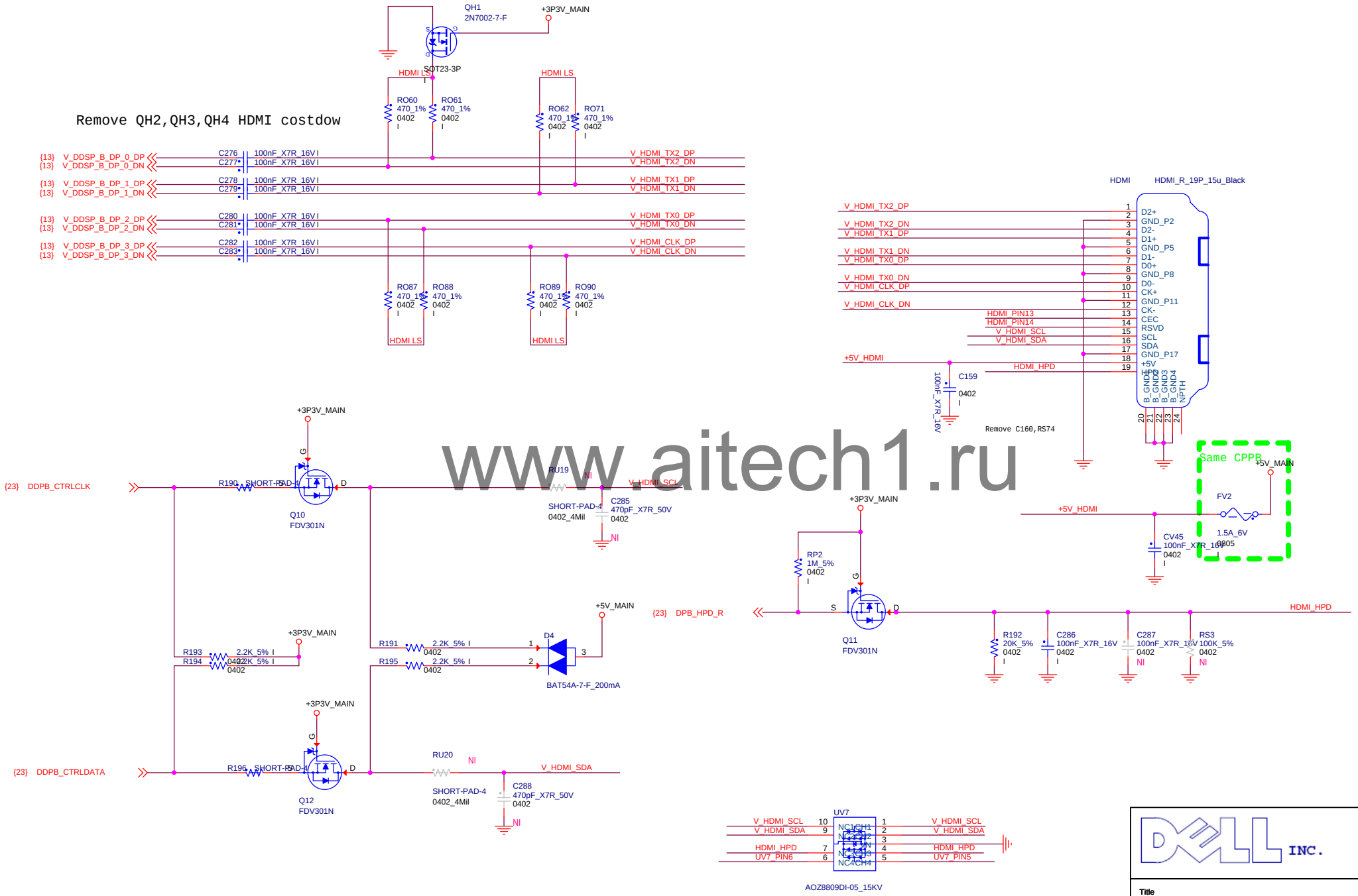
DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015



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20120521: Delete UV4 ; UV1, UV2, UV3 change to INFINEON_ESD3V3U4ULC

(13) V_DDSP_C_DP_0_DP — CV1 100nF_X7R_10V 0402 — V_DPC_TX0_DP
(13) V_DDSP_C_DP_0_DN — CV2 100nF_X7R_10V 0402 — V_DPC_TX0_DN

(13) V_DDSP_C_DP_1_DP — CV3 100nF_X7R_10V 0402 — V_DPC_TX1_DP
(13) V_DDSP_C_DP_1_DN — CV4 100nF_X7R_10V 0402 — V_DPC_TX1_DN

(13) V_DDSP_C_DP_2_DP — CV5 100nF_X7R_10V 0402 — V_DPC_TX2_DP
(13) V_DDSP_C_DP_2_DN — CV6 100nF_X7R_10V 0402 — V_DPC_TX2_DN

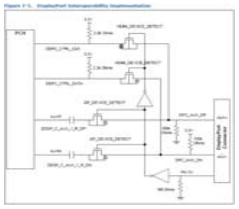
(13) V_DDSP_C_DP_3_DP — CV7 100nF_X7R_10V 0402 — V_DPC_TX3_DP
(13) V_DDSP_C_DP_3_DN — CV8 100nF_X7R_10V 0402 — V_DPC_TX3_DN
(13) V_DDSP_C_AUX_DN — CV9 100nF_X7R_10V 0402 — V_DDSP_C_AUX_DN_C
(13) V_DDSP_C_AUX_DP — CV10 100nF_X7R_10V 0402 — V_DDSP_C_AUX_DP_C

DP

Pin	Signal	Pin	Signal
1	V_DPC_TX0_DP	2	ML_LANE_0P / GND
3	V_DPC_TX0_DN	4	ML_LANE_0N / ML_LANE_1P
5	V_DPC_TX1_DP	6	GND / ML_LANE_1N
7	V_DPC_TX1_DN	8	ML_LANE_2P / GND
9	V_DPC_TX2_DP	10	ML_LANE_2N / ML_LANE_3P
11	V_DPC_TX2_DN	12	GND / ML_LANE_3N
13	V_DPC_TX3_DP	14	CONFIG1 / CONFIG2
15	V_DPC_TX3_DN	16	AUX_CH_P / GND
17	DP_P13	18	AUX_CH_N / HP_DET
19	V_DPC_AUX_DP	20	PWR_RTN / DP_PWR
21	V_DPC_AUX_DN		
22	V_DPC_HPD_SINK		
23	V_DPC_PWR		
24			

RV1 1M_5% 0402 — RV2 100K_5% 0402

DISPLAYPORT_15u_Black



+3P3V_MAIN — FV1 1.5A_6V 0805 — CV11 1uF_X5R_6.3V 0603 — CV13 470pF_X7R_50V 0402 — RV24 0_5% 0603 — FB27 300_1.5A — V_DPC_PWR — CV14 22uF_X5R_6.3V 0805

need to apply to chang to 2.5A FV1/FV2/FV3

20110211:change 2N7002DW for cost down.

FB31 47_300mA — V_DDPC_CTRL_CLK
RV28 0_5% 0603
DP_P13_POS — Q16A 2N7002DWA-7 SOT363-6P CCL=Y
V_DPC_AUX_DP
CV17 0402 NI 100nF_X7R_10V

V_DPC_AUX_DN
DP_P13_POS — Q16B 2N7002DWA-7 SOT363-6P CCL=Y
FB32 47_300mA — V_DDPC_CTRL_DATA
RV29 0_5% 0603
CV18 0402 NI 100nF_X7R_10V

Display Port Hotplug Detect

RV25 0_5% 0603
V_DPC_HPD_SINK — FB28 300_1.5A — V_DPC_HPD_SINK
+5V_MAIN — QV1 FDV301N
RV19 100K_5% 0402
CV16 0402 100nF_X7R_10V
V_DDSP_C_HPD (23)

+3P3V_MAIN — RV16 100K_5% 0402
V_DPC_AUX_DN
V_DPC_AUX_DP
RV21 100K_5% 0402

V_DPC_AUX_DP
DP_P13_INV — Q15A 2N7002DWA-7 SOT363-6P CCL=Y
V_DDSP_C_AUX_DP_C

V_DPC_AUX_DN
DP_P13_INV — Q15B 2N7002DWA-7 SOT363-6P CCL=Y
V_DDSP_C_AUX_DN_C

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+3P3V_MAIN — RV7 2.2K_5% 0402 — RV8 2.2K_5% 0402 — +3P3V_MAIN
(23) V_DDPC_CTRL_CLK — V_DDPC_CTRL_CLK
(23) V_DDPC_CTRL_DATA — V_DDPC_CTRL_DATA

+19V_MAIN — RV9 10K_5% 0402
FB33 600_200mA — DP_P13_INV
RV39 0_5% 0603
CV21 100nF_X7R_16V 0402

RV11 10K_5%
QV2A 2N7002DWA-7 SOT363-6P CCL=Y
QV2B 2N7002DWA-7 SOT363-6P CCL=Y

+19V_MAIN — RV10 10K_5% 0402
RV23 10K_5%

DP_P13 DP_P13 — FB29 600_200mA — RV39 0_5% 0603 — RV14 1M_5% 0402 — RV13 8.2K_5% 0402 — CV15 0402 100nF_X7R_10V — CV19 0402 100nF_X7R_10V

FB30 600_200mA — DP_P13_POS — RV22 0_5% 0603 — CV20 100nF_X7R_16V 0402

DELL INC.

Title: Display Port 1

DWG NO: D7 Micro

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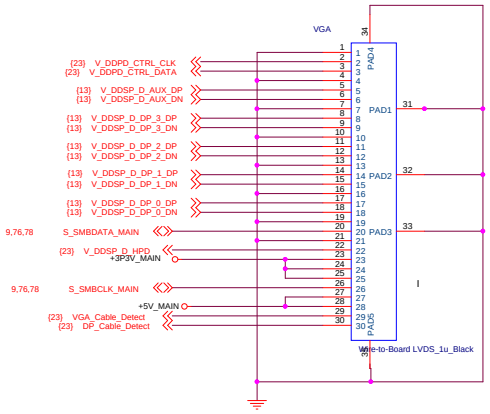

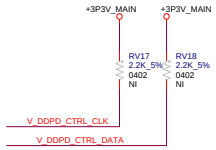

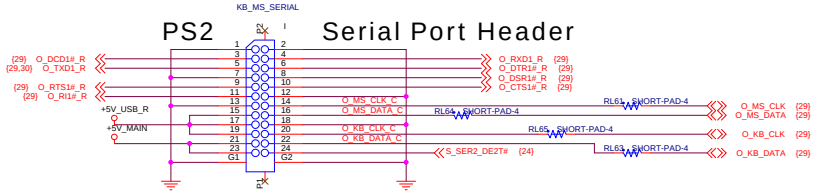

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DELL INC.

Title: **Display Port 2**

DWG NO: ***D7 Micro***

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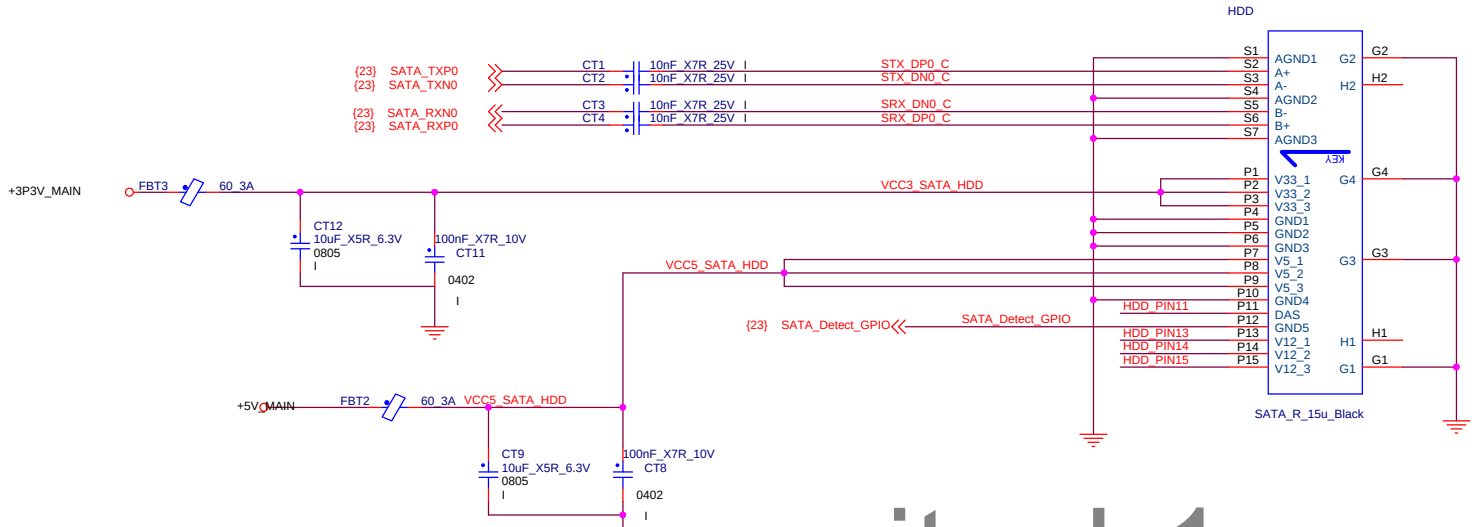
HDD SATA CONNECTOR



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DELL INC.

Title

SATA Conn

DWG NO

D7 Micro

Rev

X01

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Rear USB 2.0 CONNECTOR

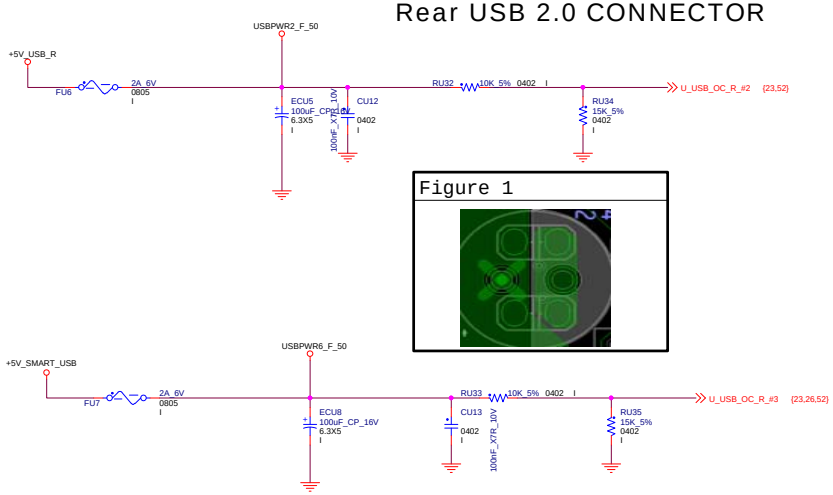
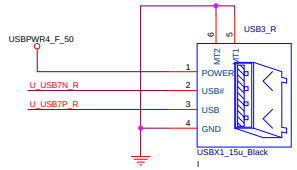
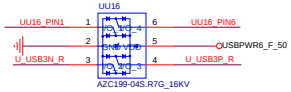
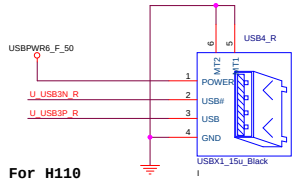


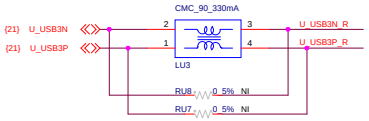
Figure 1



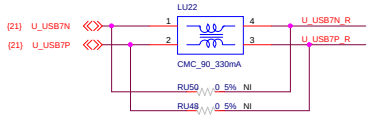




For H110



Place ESD Close to Connector



Rear USB 3.0 CONNECTOR

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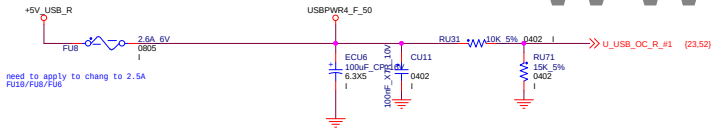
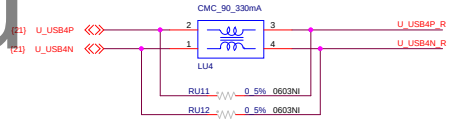
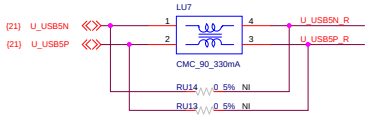
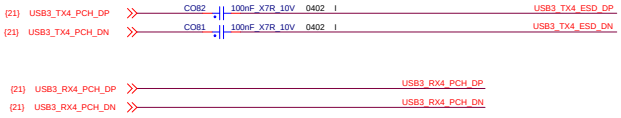
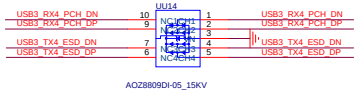
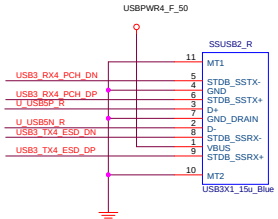


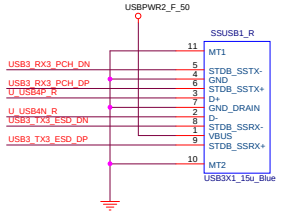




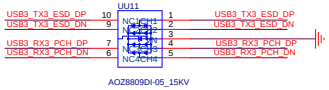








Place ESD Close to Header



DELL INC.

Title: **Rear USB3.0**

DWG NO: *D7 Micro*

Rev: X01

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DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

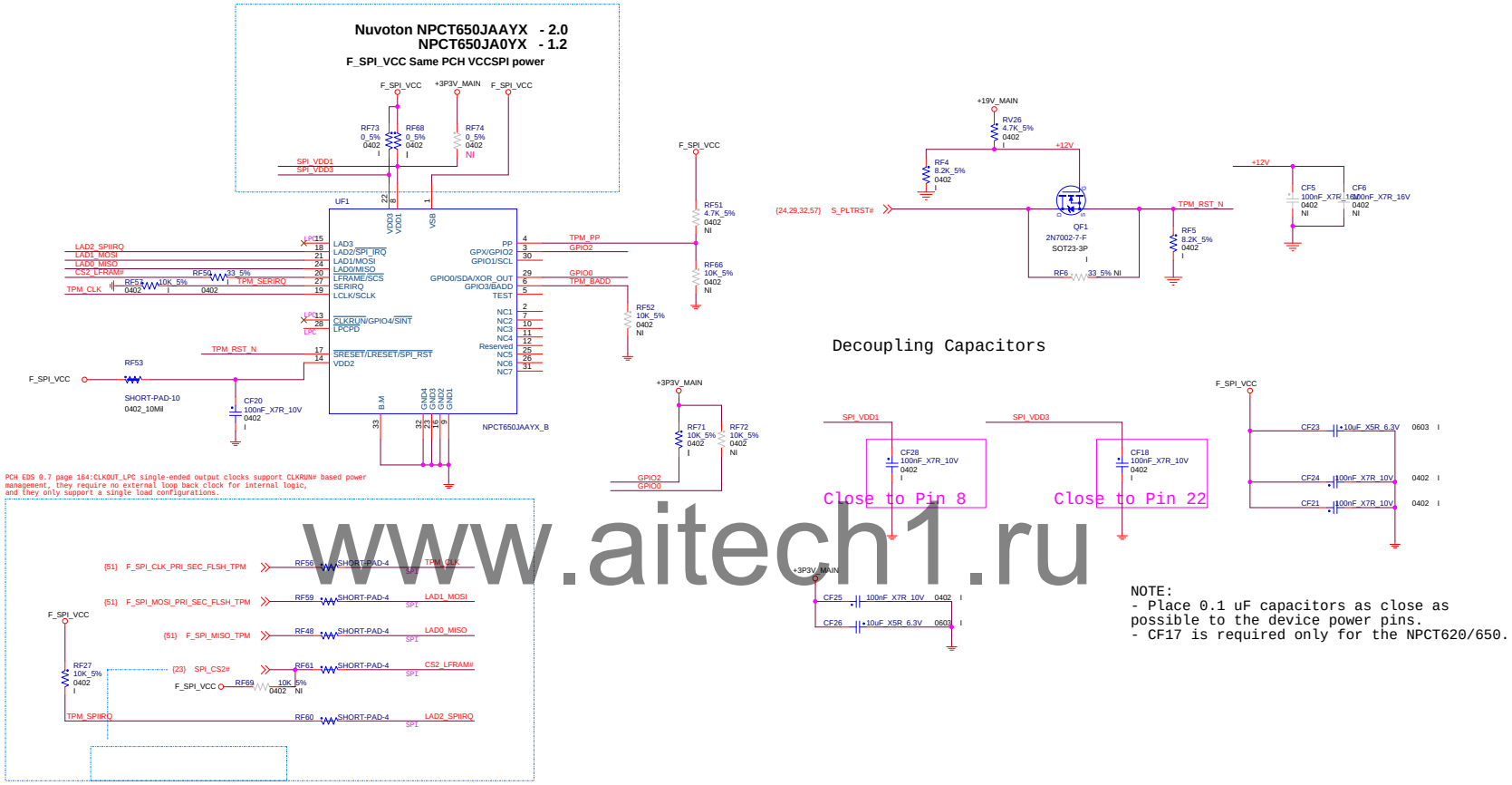
D7 Micro

Rev

X01

Date: Monday, August 03, 2015

TPM



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NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- CF17 is required only for the NPCT620/650.

DELL INC.

Title: TPM

DWG NO: D7 Micro

Rev: X01

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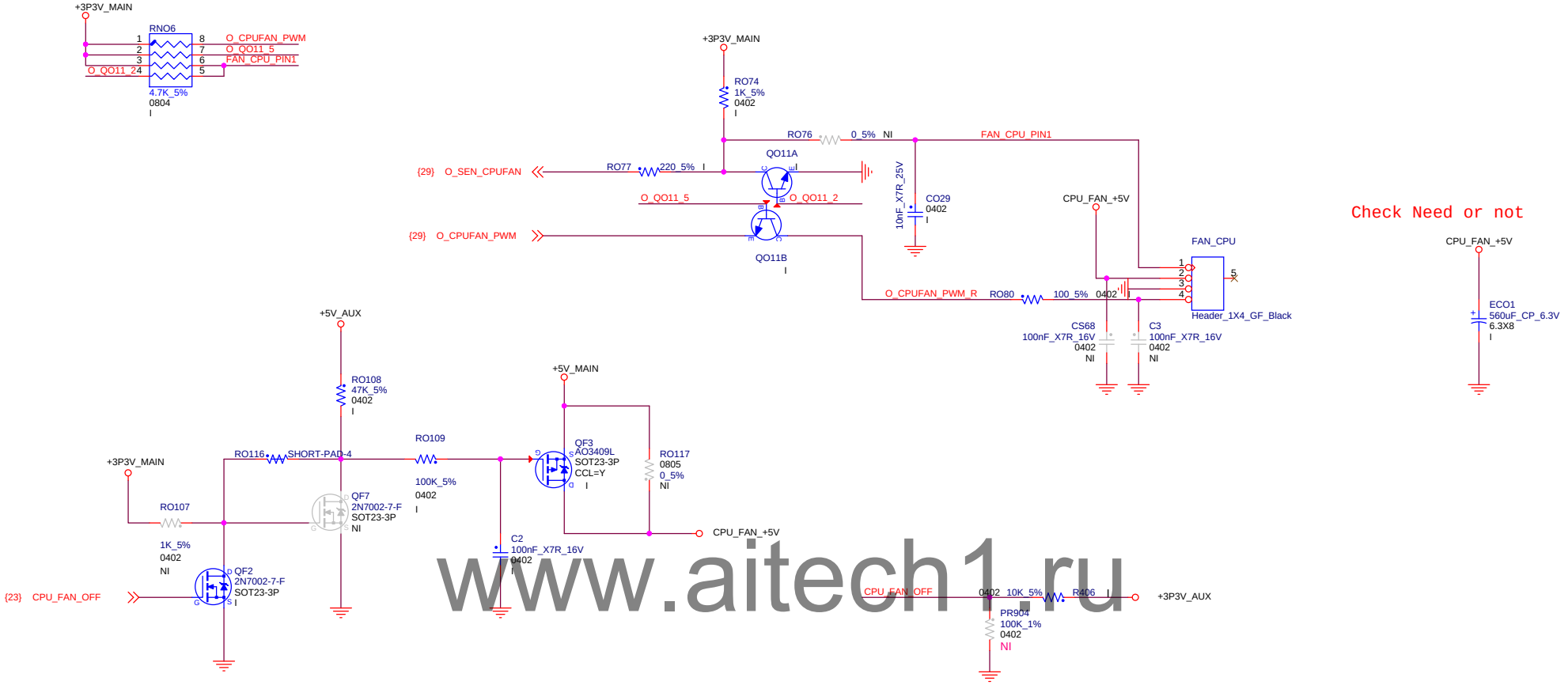
CPU Fan



www.aitech1.ru

SYS Fan

LABEL

BIOS_LICENCE
BIOS LABLE
NI

20120322 follow D4 change module fron EMI to Label

DELL INC.

Title: FAN

DWG NO: D7 Micro

Rev: X01

Date: Monday, August 03, 2015 Sheet 46 of 83

www.aitech1.ru

DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015

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DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015

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DELL INC.

Title

CPU-1: DDR3_CHA & B

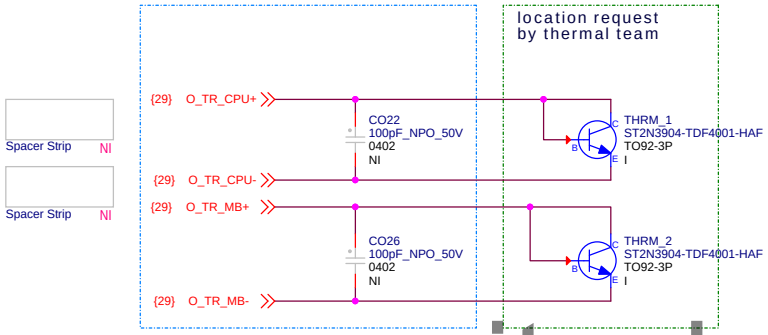
DWG NO

D7 Micro

Rev

X01

Date: Monday, August 03, 2015



20100210: Swap CO24 and CO14 layout location
Swap CO23 and CO17 layout location

20100309: Dummy CO17,CO14

20100311: THRM2 reference name rename to THRM_1 , THRM3 reference name rename to THRM_2 , follow Dell PIG1.2

20040523use Holder and 3904 DIP for Thermal request

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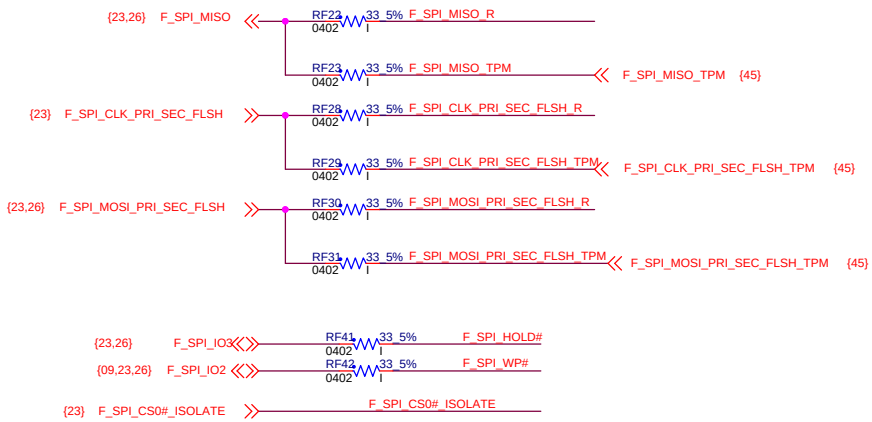
DELL INC.

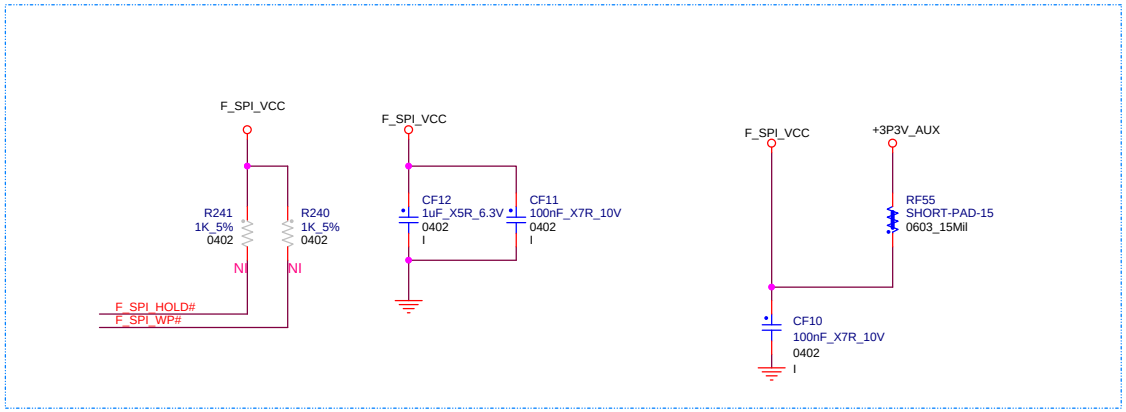
Title
Thermal Sensor

DWG NO
D7 Micro

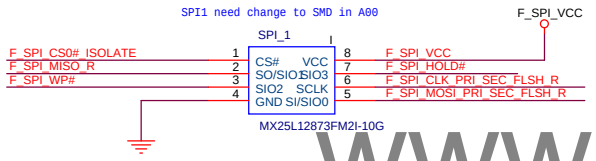
Rev
X01

Date: Monday, August 03, 2015 Sheet 50 of 83

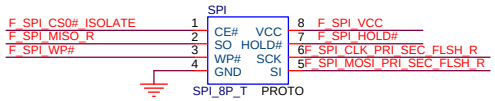




SPI_8MB



20140506: SPI1 Change to WINBOND_W25Q128FVSIQ



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DELL INC.

Title
SPI

DWG NO
D7 Micro

Rev
X01

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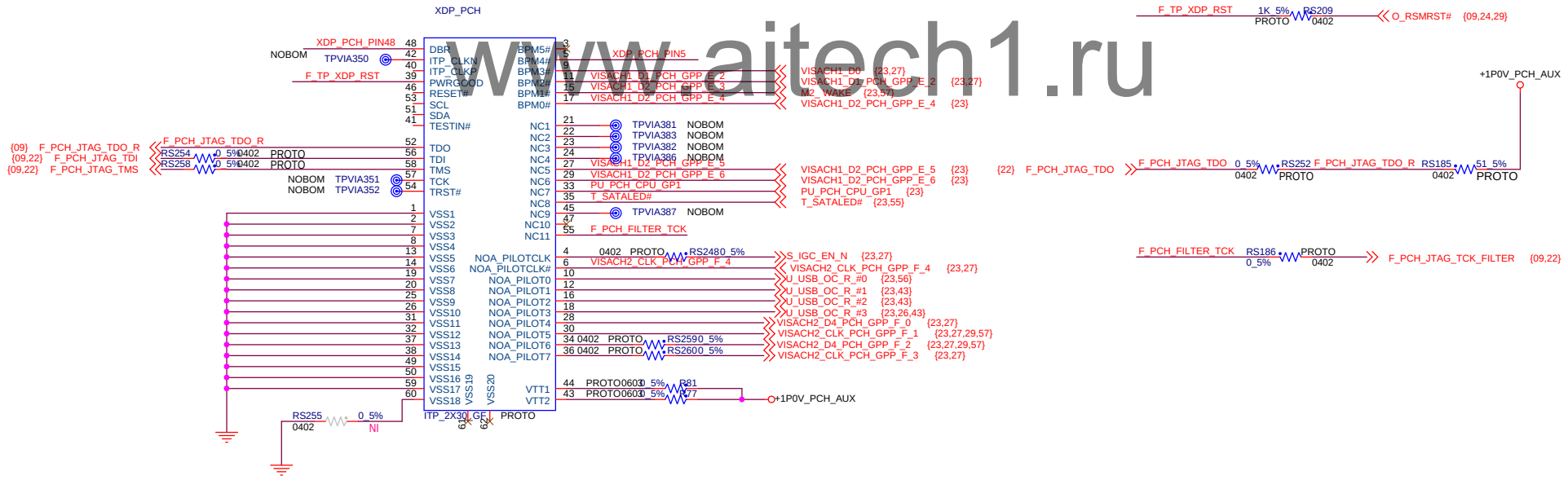
XDP Connector - PCH



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DELL INC.

Title

XDP

DWG NO

D7 Micro

Rev **X01**

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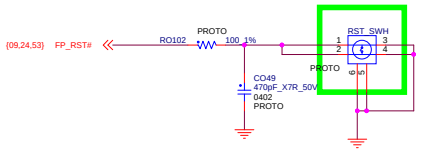
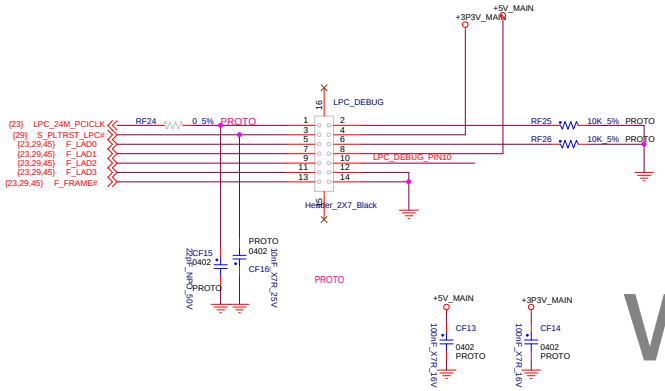
Power Bottom

Remove PWR_SWH

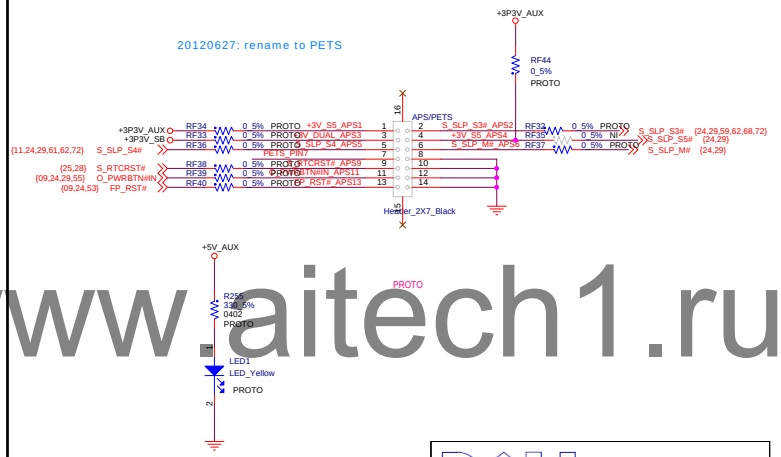
Reset Bottom



LPC DEBUG



APS Connector



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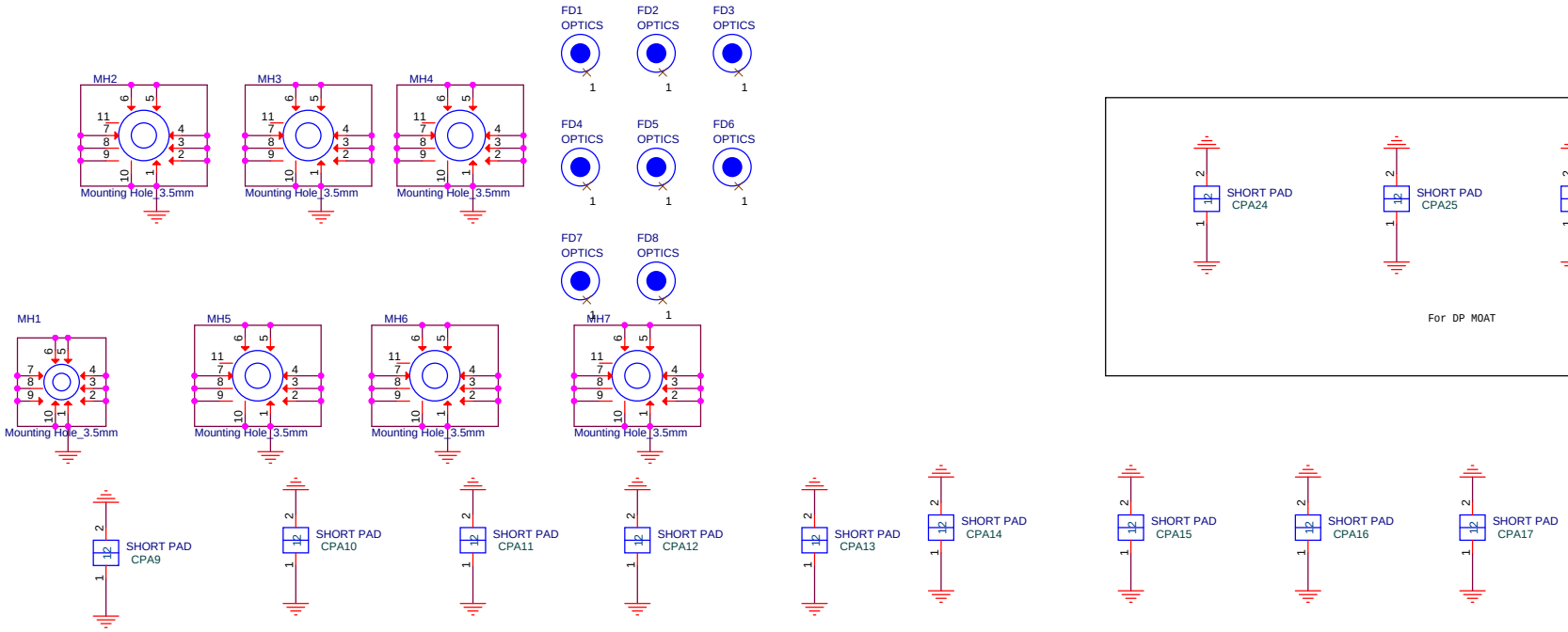
DELL INC.

Title: **Pilot Run Conn**

DWG NO: *D7 Micro*

Rev: X01

Date: Monday, August 03, 2015 Sheet 53 of 83



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DELL INC.

Title

EMI

DWG NO

D7 Micro

Rev **X01**

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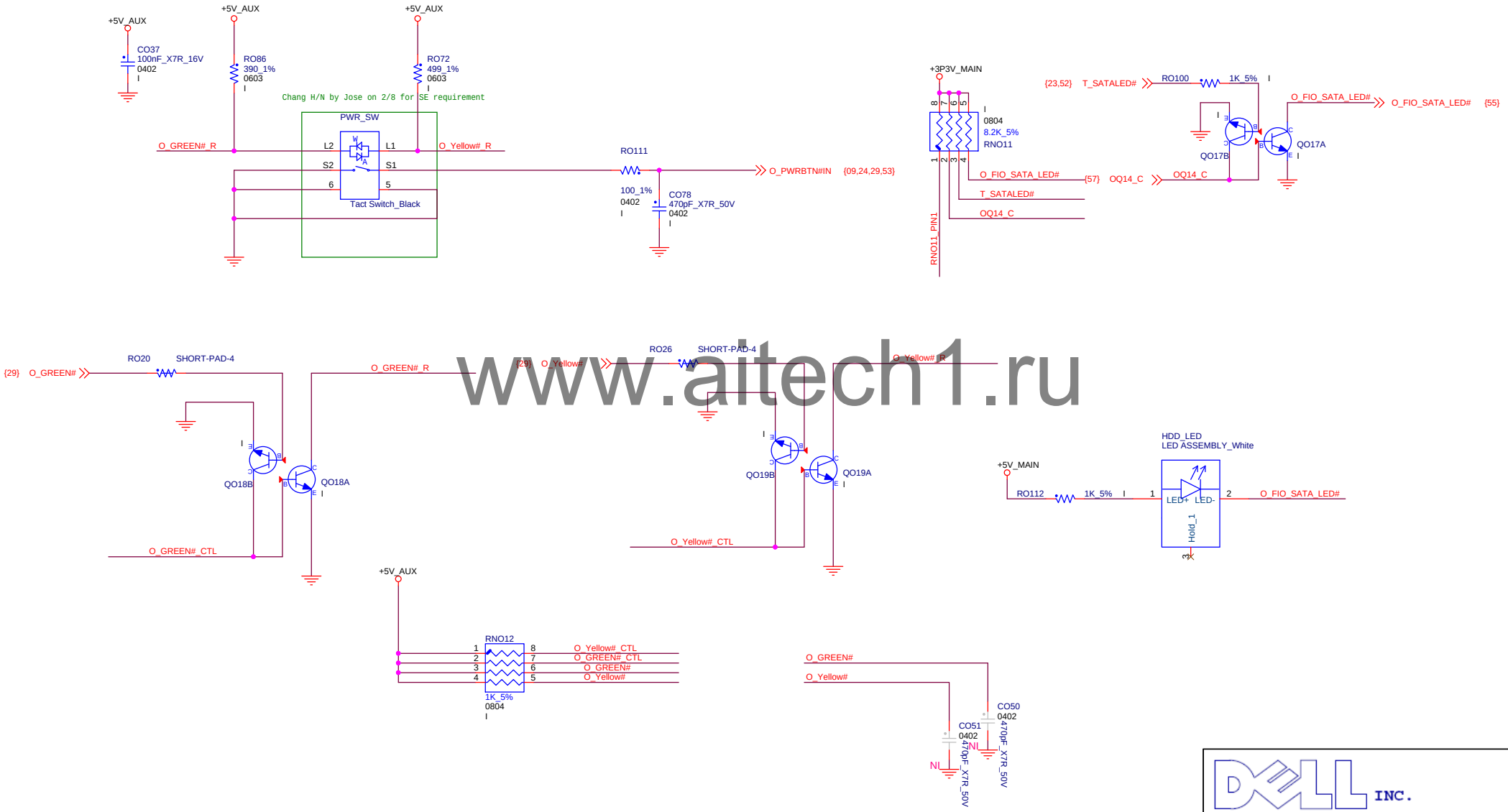
FRONTPANEL Header



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DELL INC.

Title

Front_Panel

DWG NO

D7 Micro

Rev **X01**

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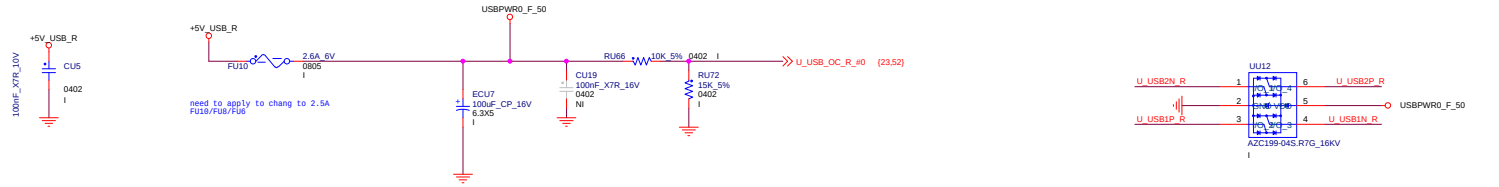
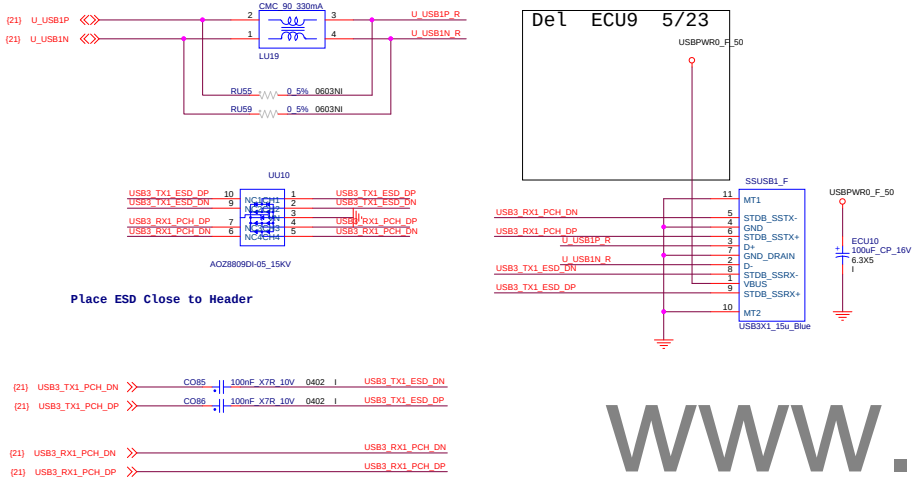
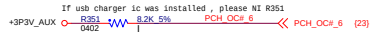
Front USB Connector







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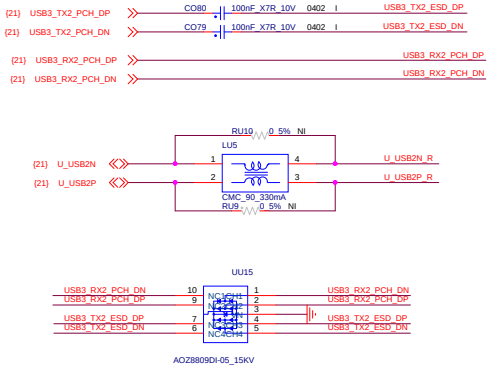

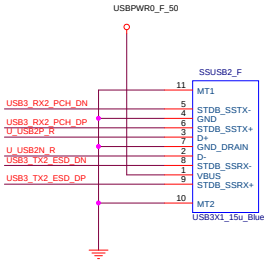

DELL INC.

Title: **TBD**

DWG NO: ***D7 Micro***

Rev: **X01**

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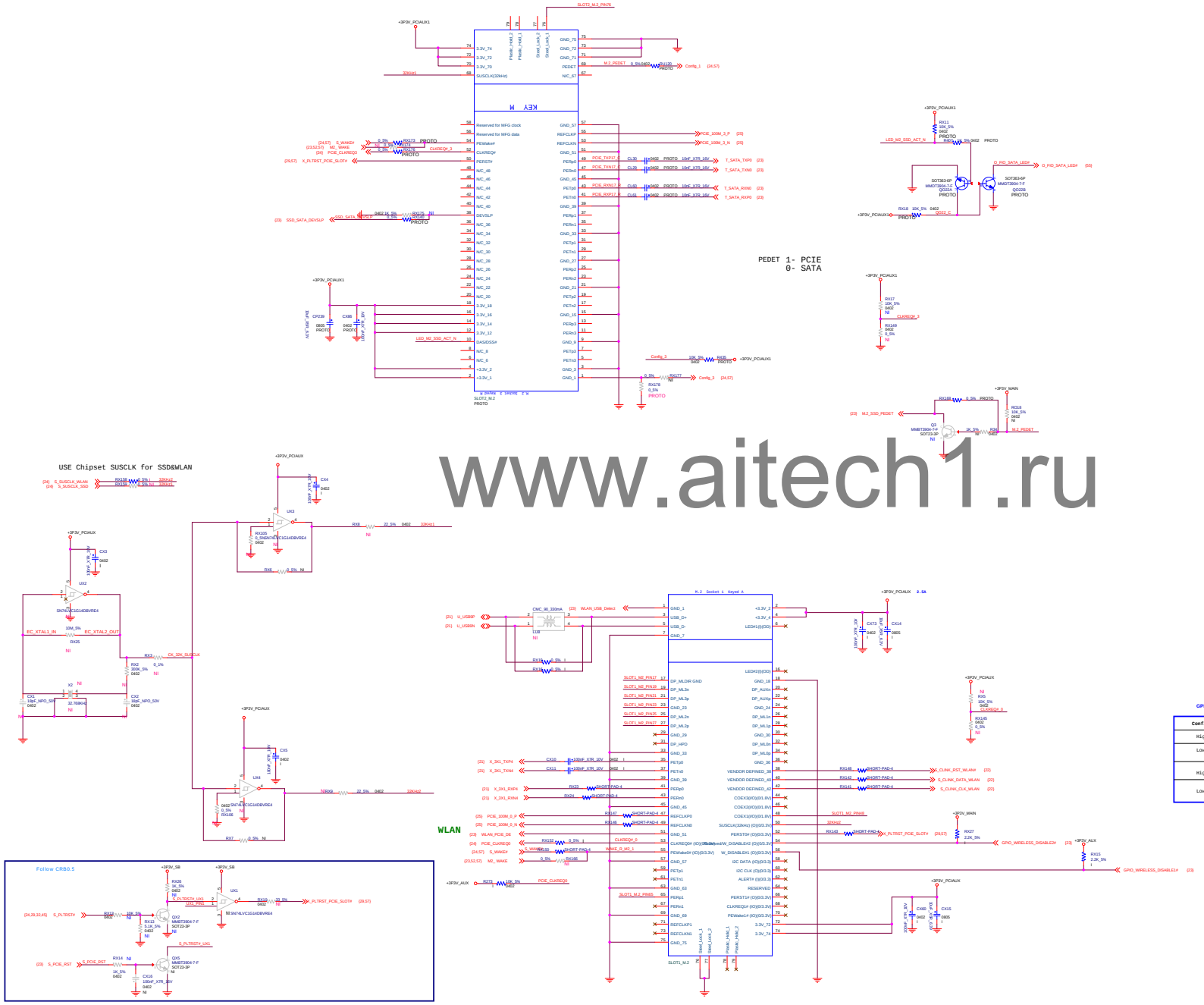
STATE#	CONFIG_0: Pin21	CONFIG_1: Pin69	CONFIG_2: Pin75	CONFIG_3: Pin1	Module Type
0	GND	GND	GND	GND	SSD – SATA
1	GND	NC	GND	GND	SSD - PCIe
8	NC	GND	GND	GND	WWAN
14	NC	GND	NC	NC	DDP|HCA - PCIe
15	NC	NC	NC	NC	No Module Present

Input				Output		Module Type
CONFIG_0 Pin21	CONFIG_1 Pin69	CONFIG_2 Pin75	CONFIG_3 Pin1	Output GP105	Output GP107	
PCH_GPIO_50	PCH_GPIO_52	PCH_GPIO_53	PCH_GPIO_54	SIO_GP105	SIO_GP107	
L	L	L	L	H	H	SSD_SATA
L	NC	L	L	L	L	SSD-PCIe
NC	L	L	L		WAN	WAN
NC	L	NC	NC	L	L	DDP|HCA-PCIe



Config_0	Config_1	GPIO49/GPIO16	Interface
High	High	Low	PCIE
Low	High	Low	PCIE
High	Low	Low	PCIE
Low	Low	High	SATA

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DELL INC.

Title: Mini PCIe/MSATA

DWG NO: D7 Micro

Rev: X01

Date: Monday, August 09, 2010

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DELL INC.

Title

CPU-1: DDR3_CHA & B

DWG NO

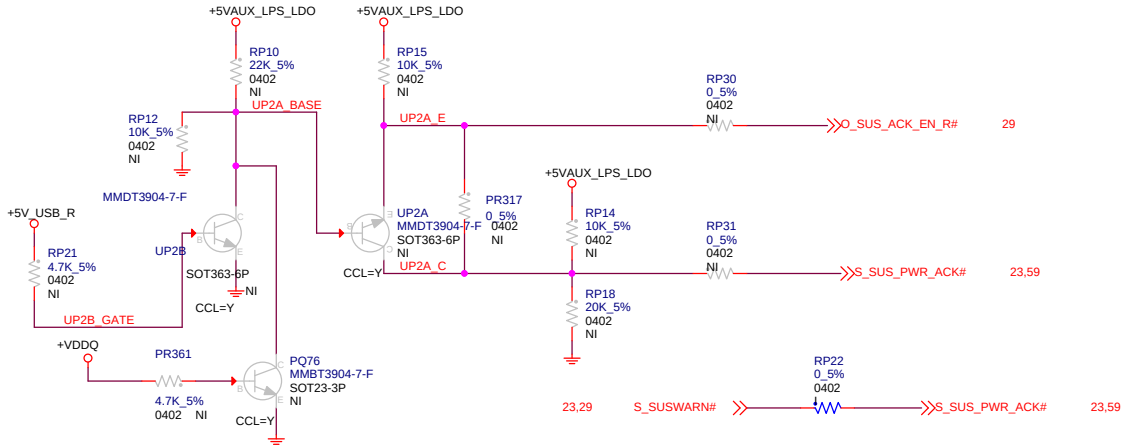
D7 Micro

Rev

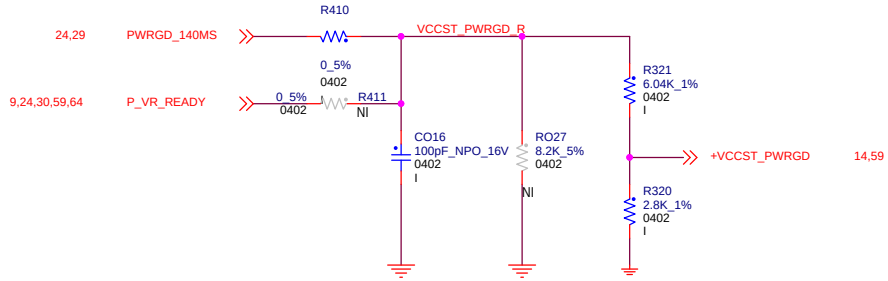
X01

Date: Monday, August 03, 2015

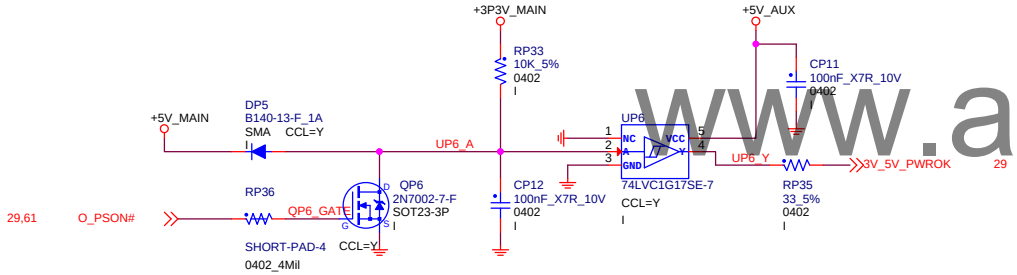
Power Sequence



VCCST_PWRGD/PCH_PWROK



Vcore Enable



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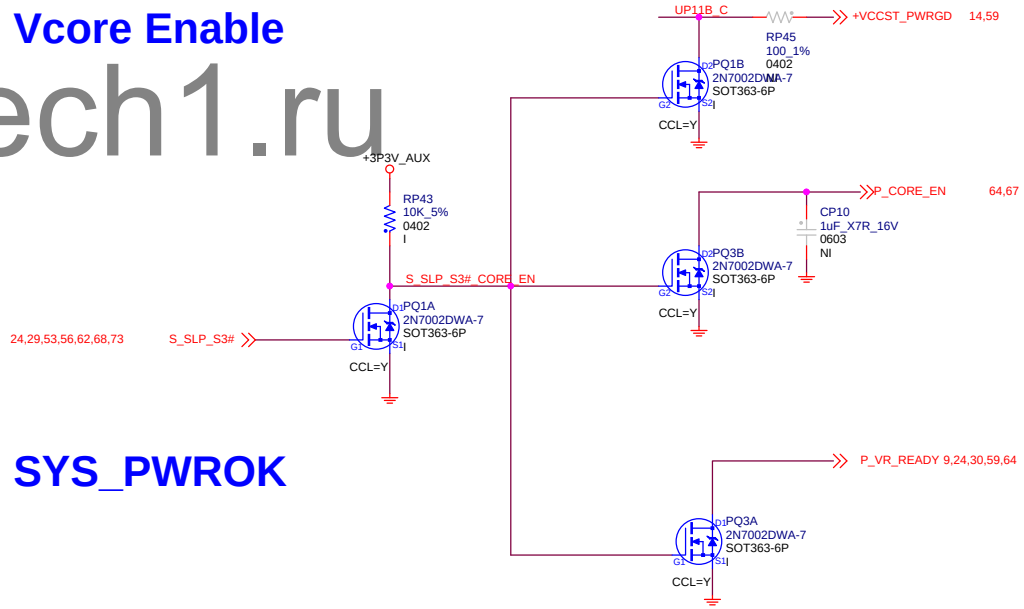

SYS_PWROK

DELL INC.

Title

Power Sequence

DWG NO

D7 Micro

Rev

X01

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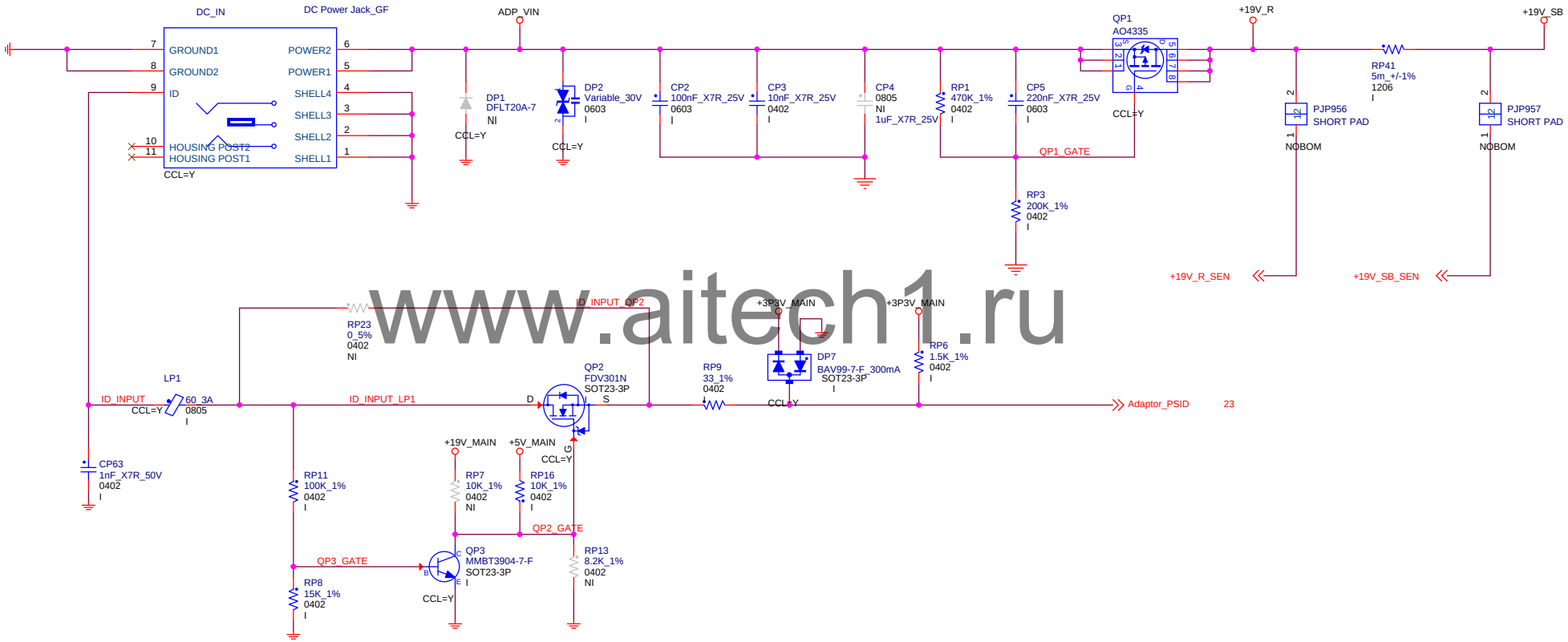
ATX POWER CONNECTOR



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DELL INC.

Title

Power Conn

DWG NO

D7 Micro

Rev

X01

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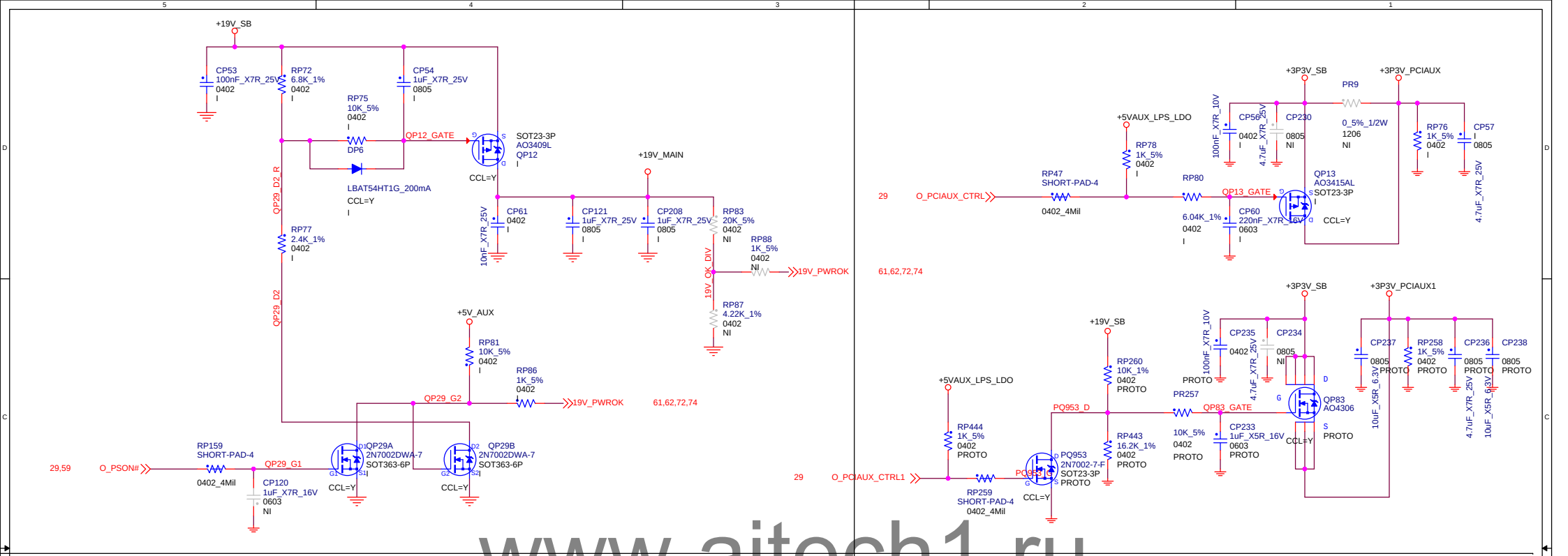

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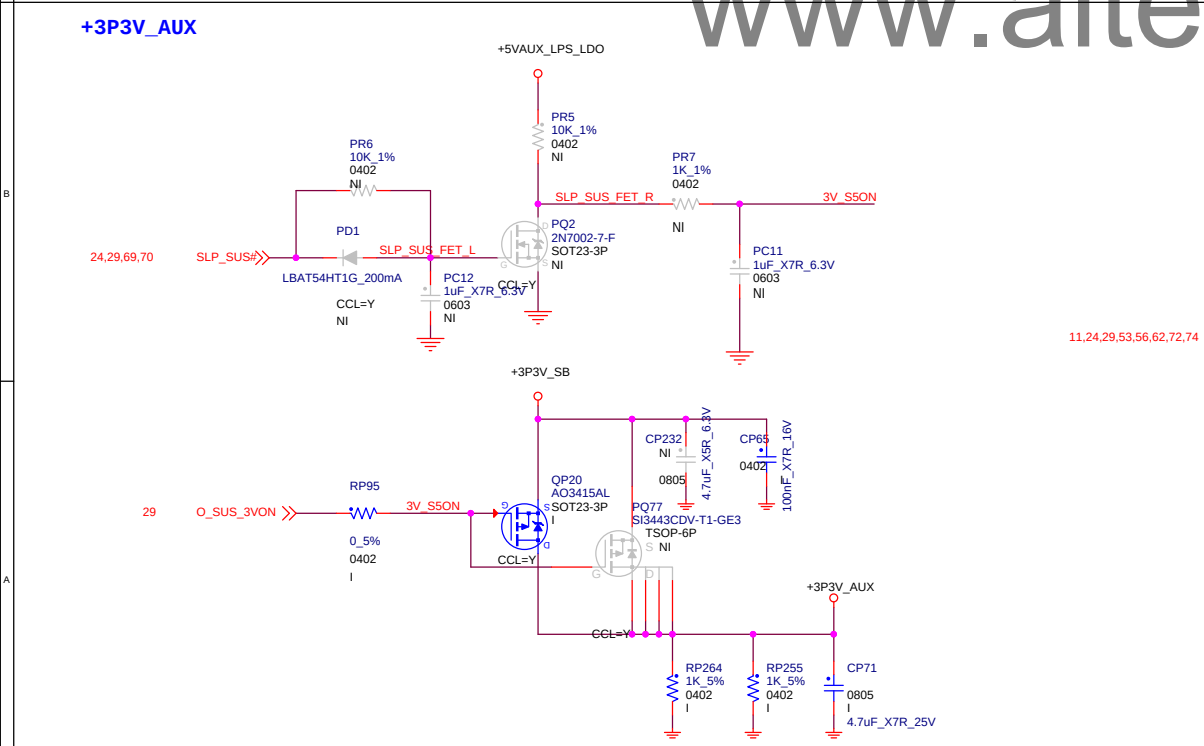
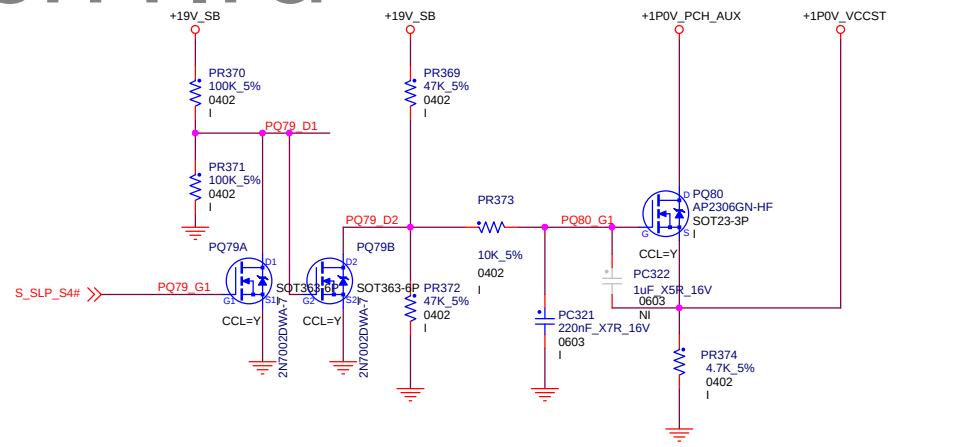
+3P3V_AUX



+1P0V_VCCST



DELL INC.

Title

5VSB/+3V_DUAL

DWG NO **D7 Micro** Rev **X01**

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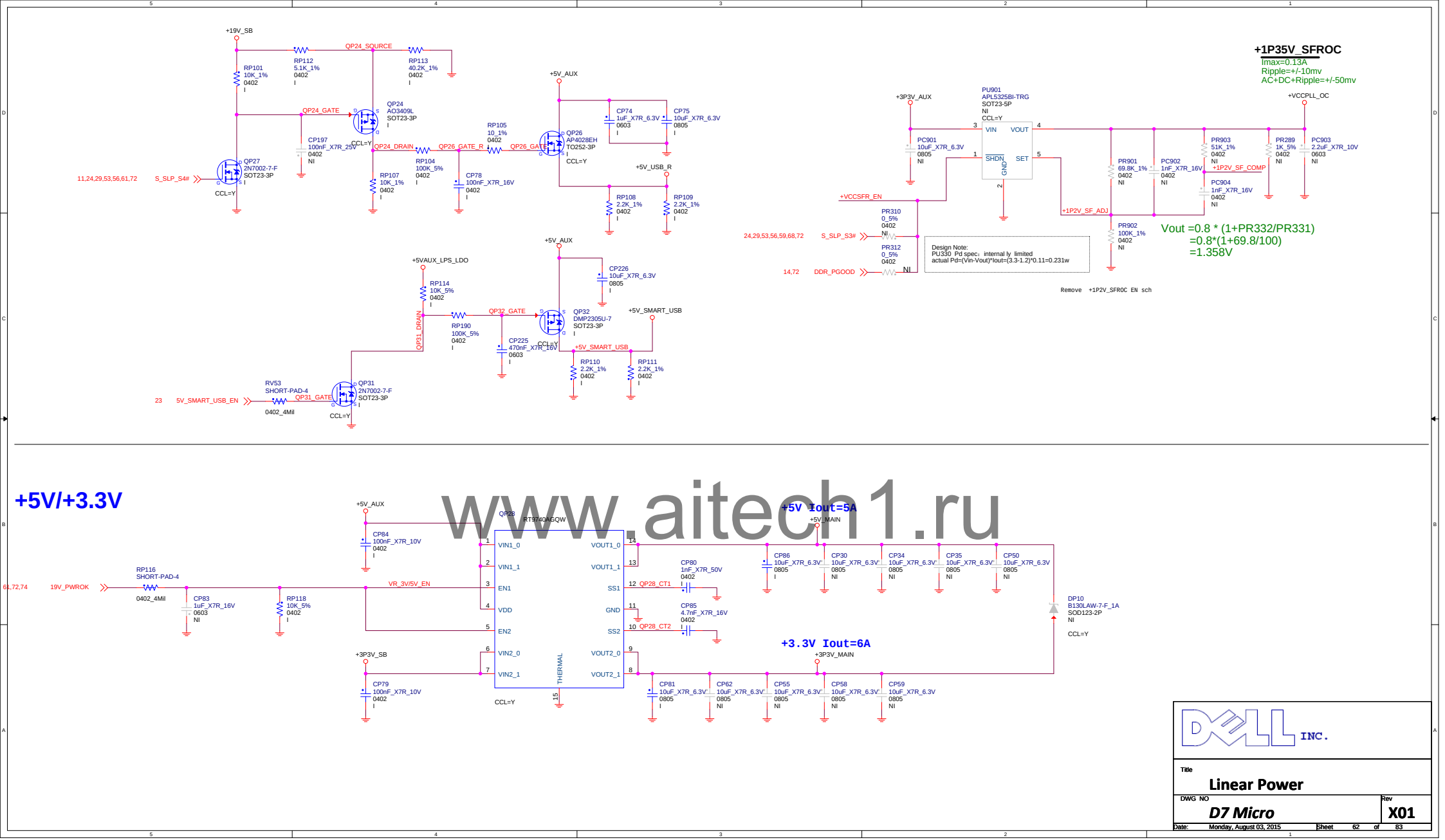

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DELL INC.

Title
Linear Power

DWG NO
D7 Micro

Rev
X01

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DELL INC.

Title

DWG NO

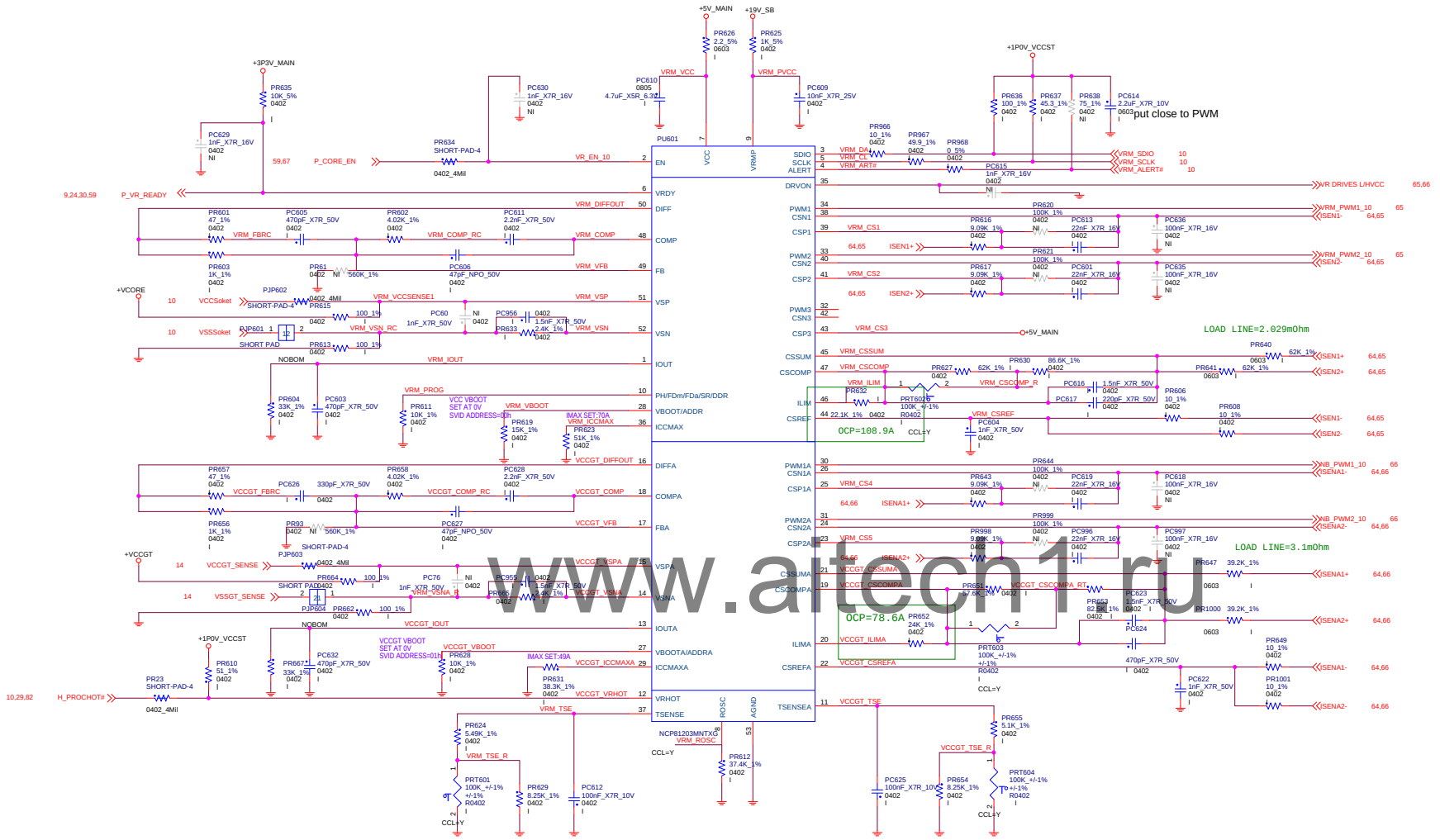
D7 Micro

Rev

X01

Date: Monday, August 03, 2015

VCORE_Controller



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DELL INC.

Title: VCORE

DWG NO: D7 Micro

Rev: X01

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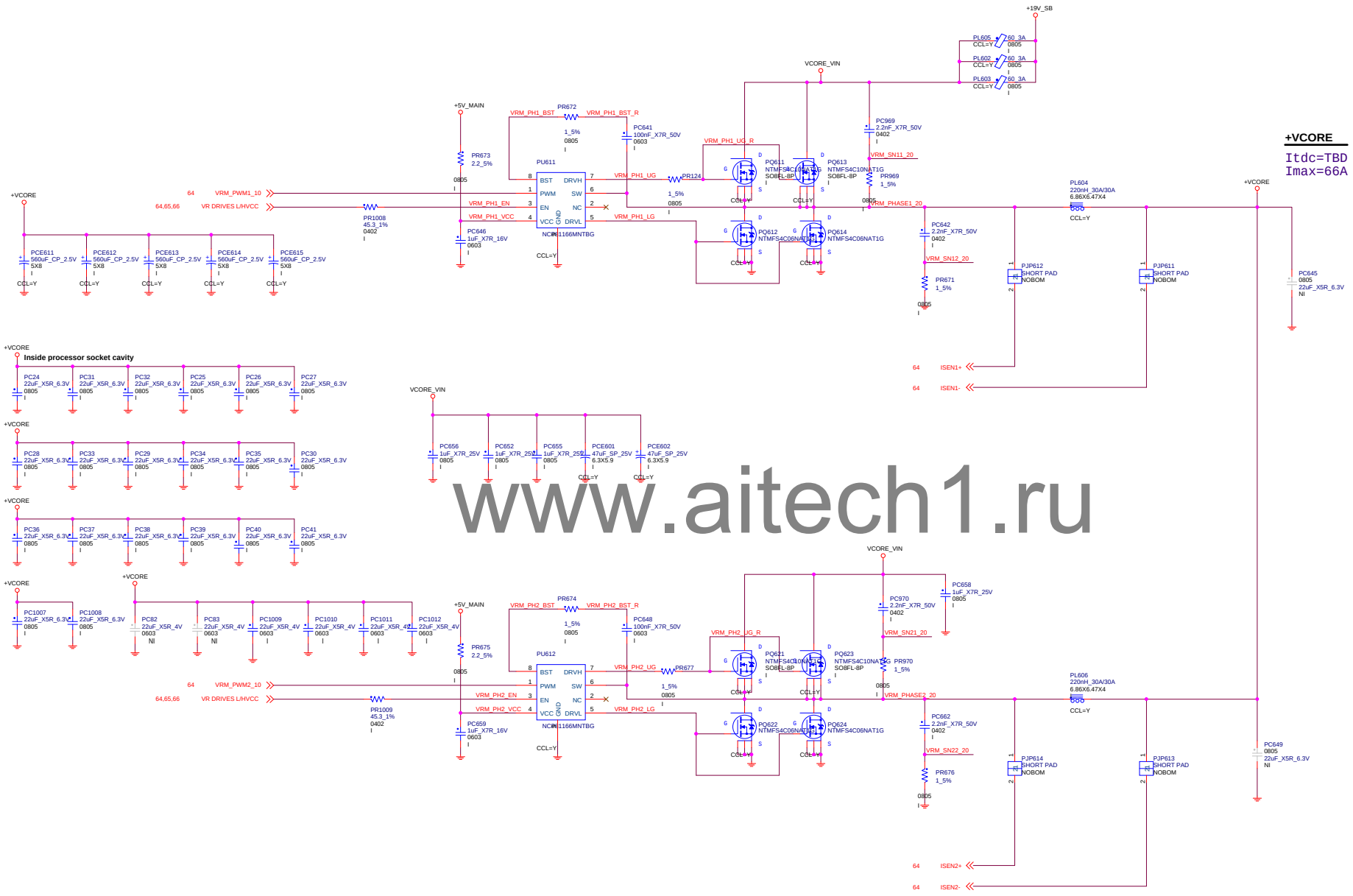
VCORE_Driver



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DELL INC.

Title: VCORE PHASE12

DWG NO: D7 Micro

Rev: X01

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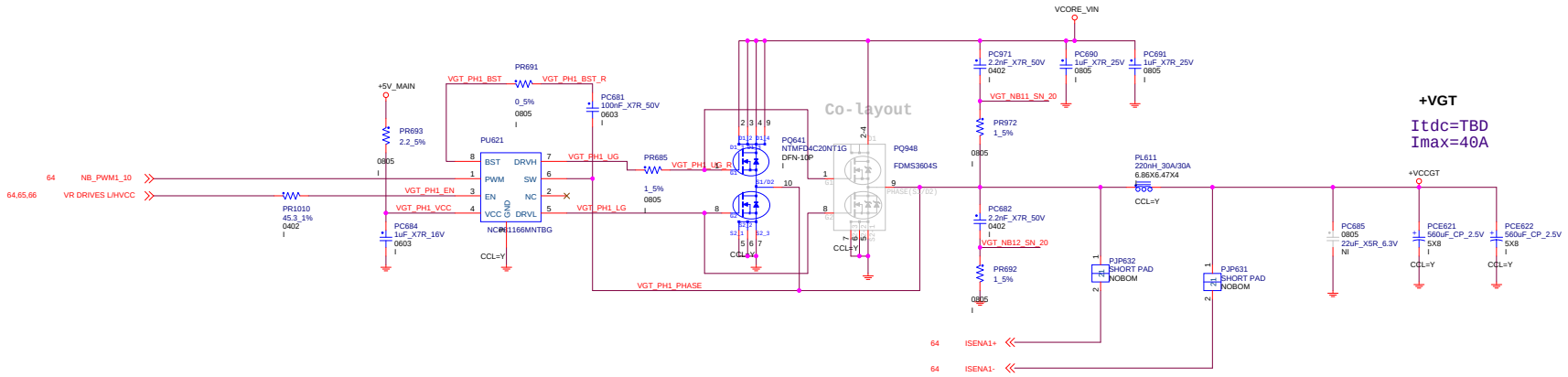
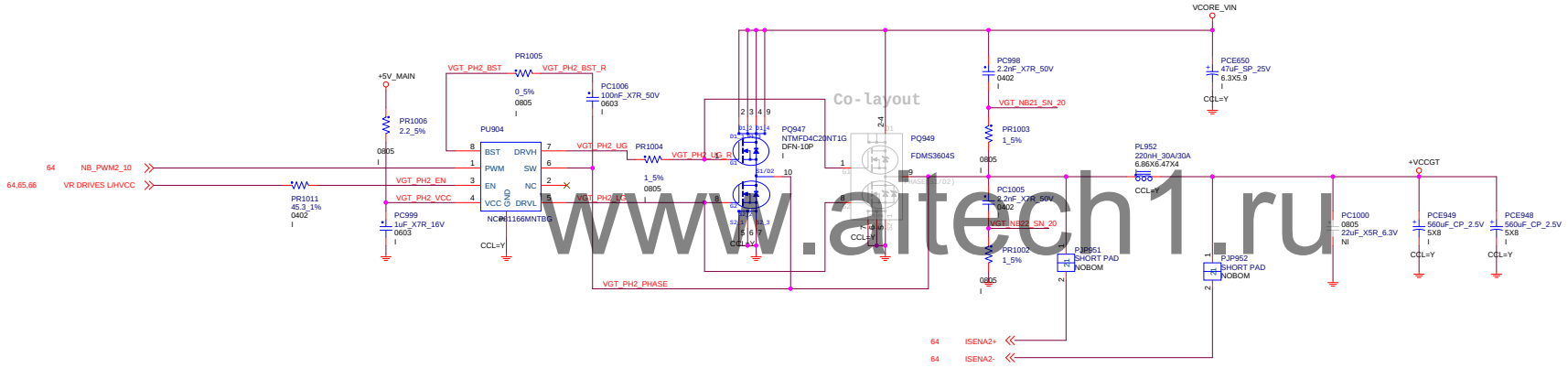
VCORE_Driver



+VGT

Itdc=TBD
Imax=40A



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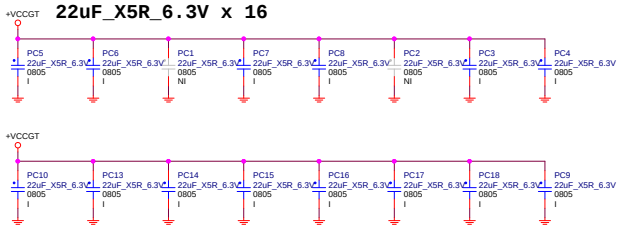
22uF_X5R_6.3V x 16



DELL INC.

Title
VGT PHASE12

DWG NO
D7 Micro

Rev
X01

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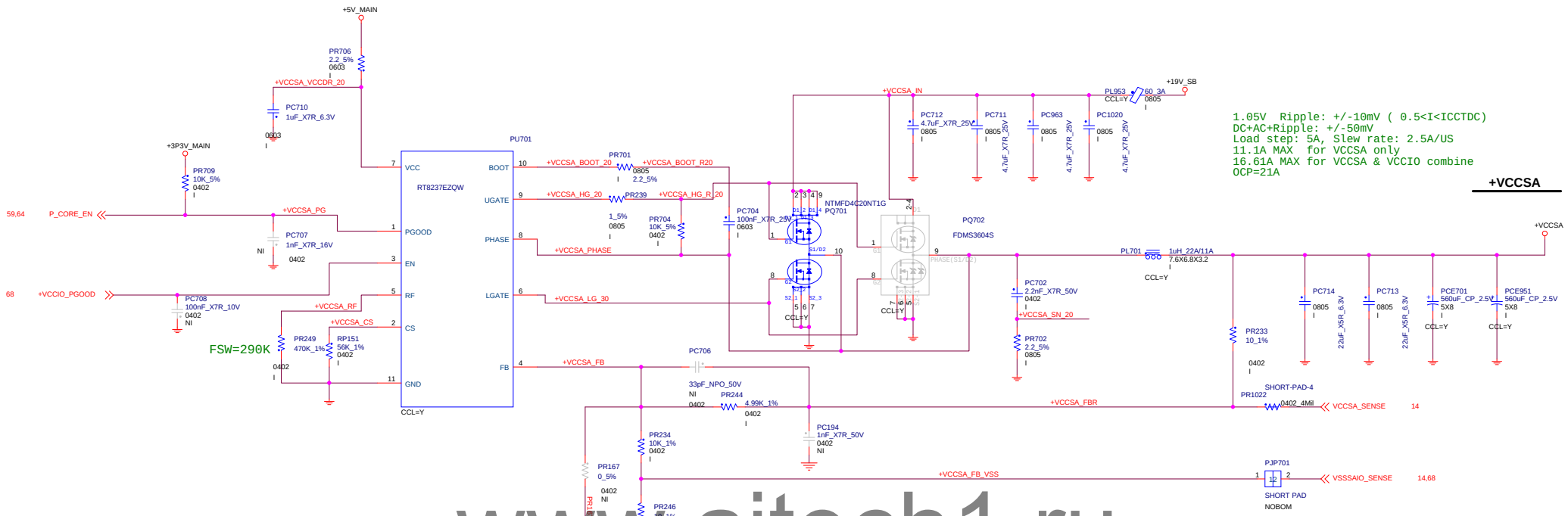

1.05V Ripple: +/-10mV (0.5<I<ICCTDC)
DC+AC+Ripple: +/-50mV
Load step: 5A, Slew rate: 2.5A/US
11.1A MAX for VCCSA only
16.61A MAX for VCCSA & VCCIO combine
OCP=21A

+VCCSA

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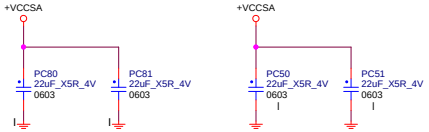
22uF_X5R_6.3V x 2 (CPU CAVITY)



DELL INC.

Title: VCCSA

DWG NO: D7 Micro

Rev: X01

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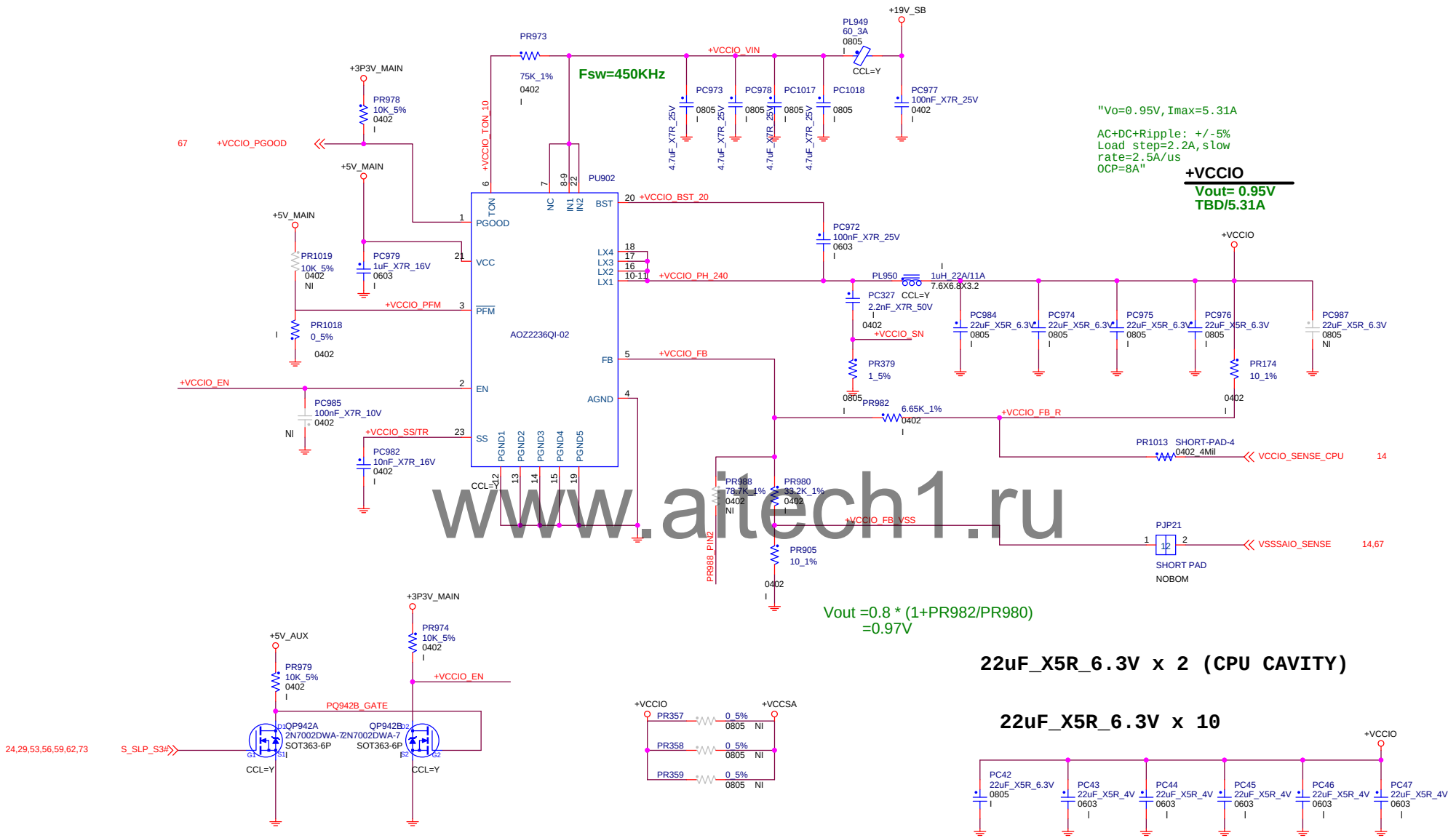

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DELL INC.

Title
VCCIO

DWG NO
D7 Micro

Rev
X01

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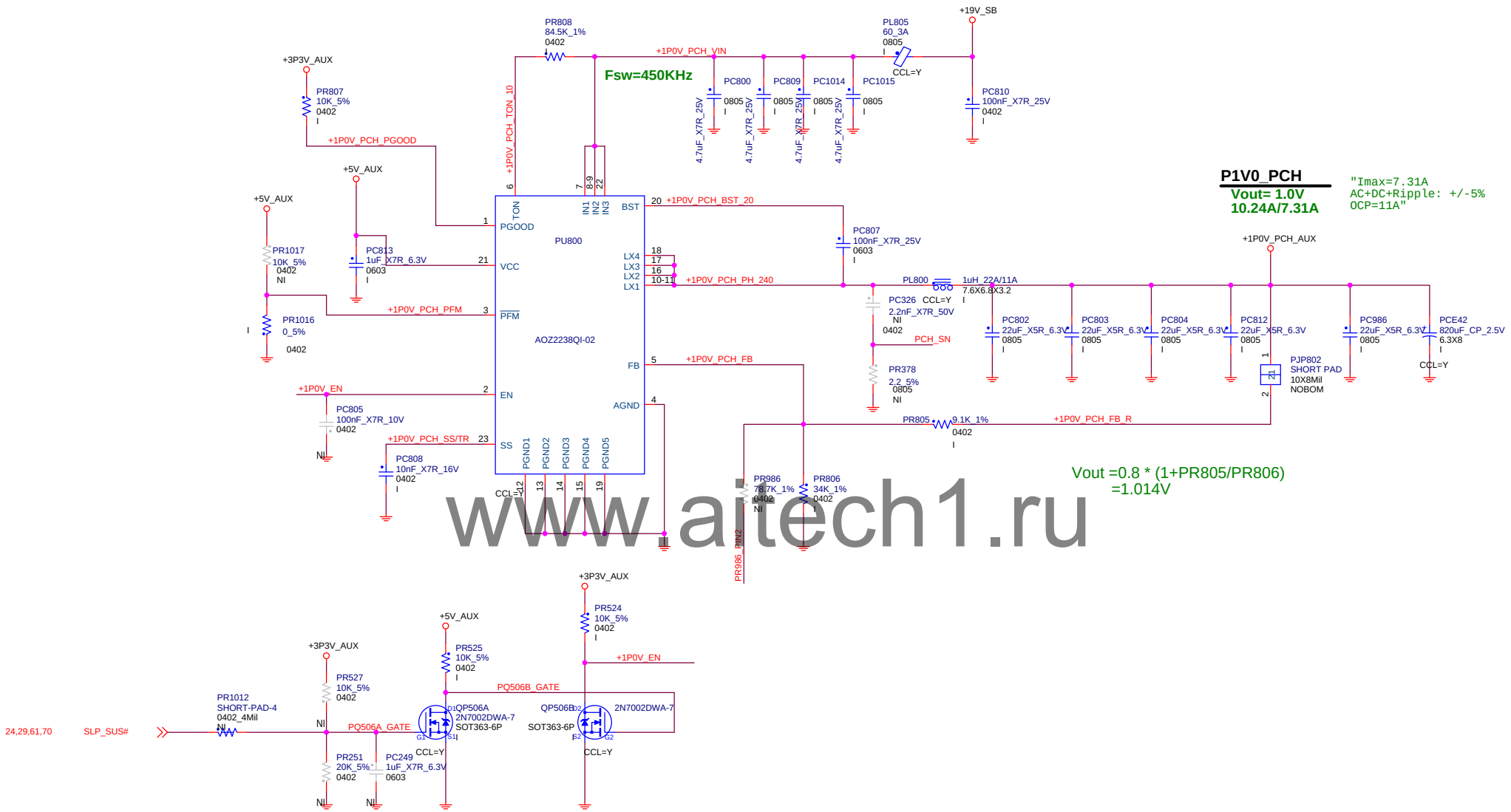

DELL INC.

Title

+1P0V_PCH

DWG NO **D7 Micro** Rev **X01**

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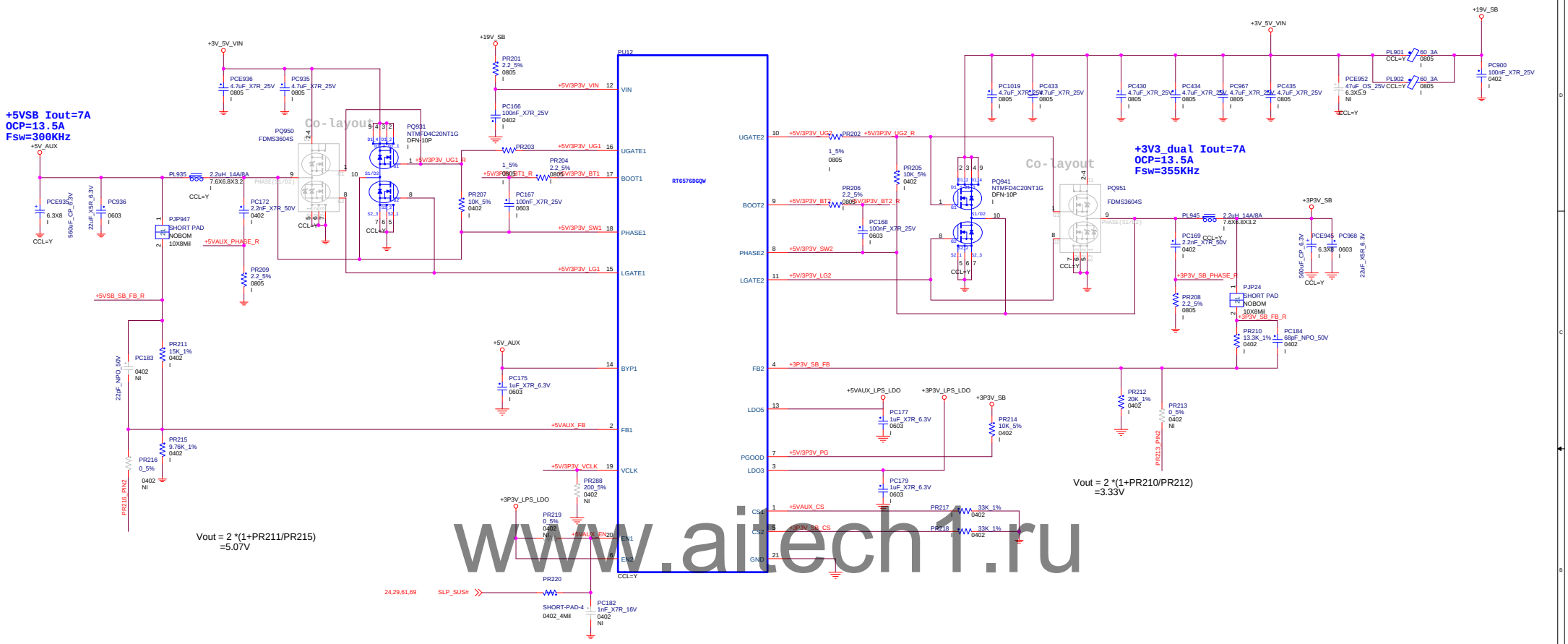

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DELL INC.

Title: +5VSB/+3V_DUAL

DWG NO: D7 Micro

Rev: X01

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DELL INC.

Title

VCORE PHASE3

DWG NO

D7 Micro

Rev

X01

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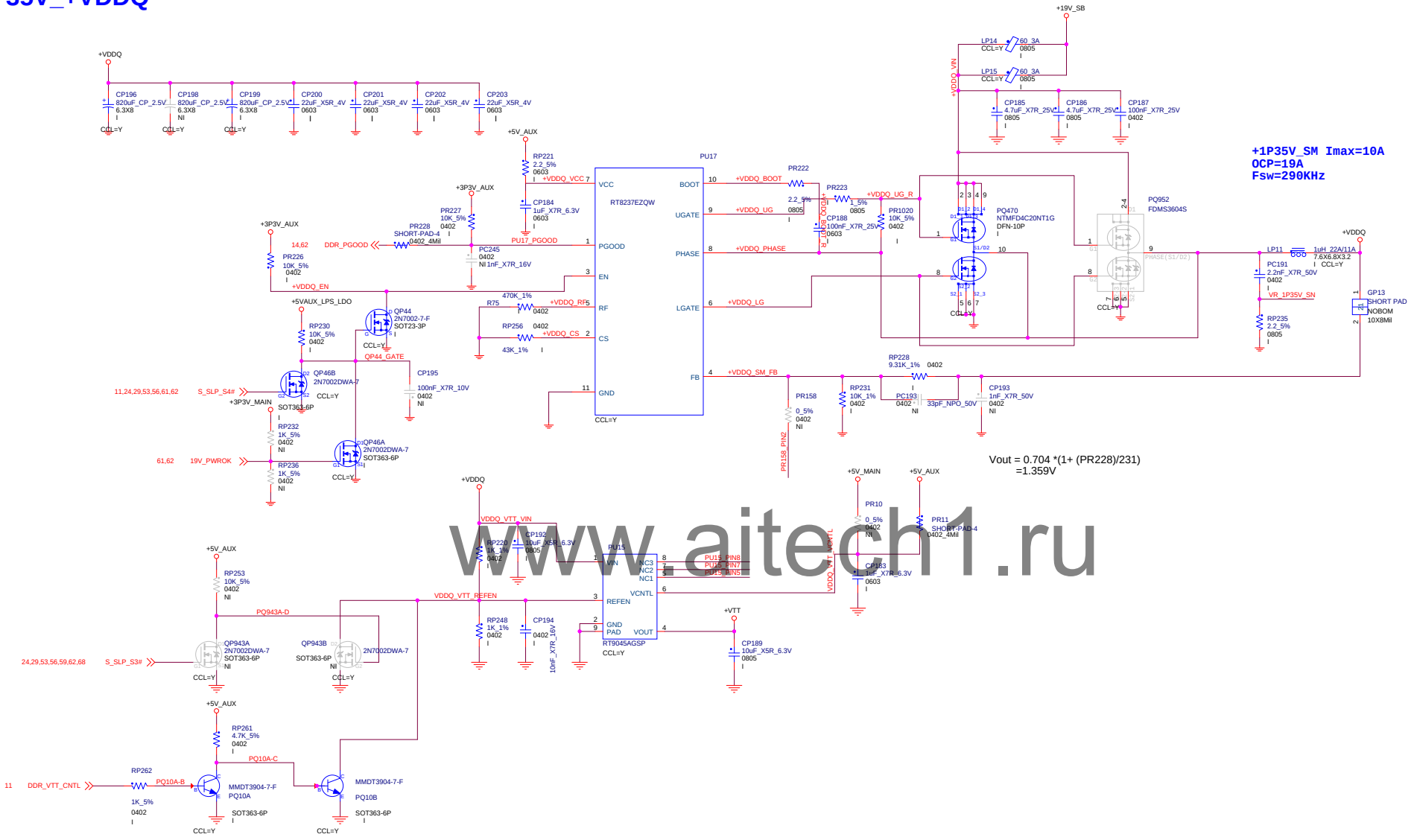
+1P35V_+VDDQ



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DELL INC.

Title
DDR

DWG NO
D7 Micro

Rev
X00

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Title

DDR

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D7 Micro

Rev

X01

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Title

+1P2V_SFROC

DWG NO

D7 Micro

Rev

X01

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Title

CPU-1: DDR3_CHA & B

DWG NO

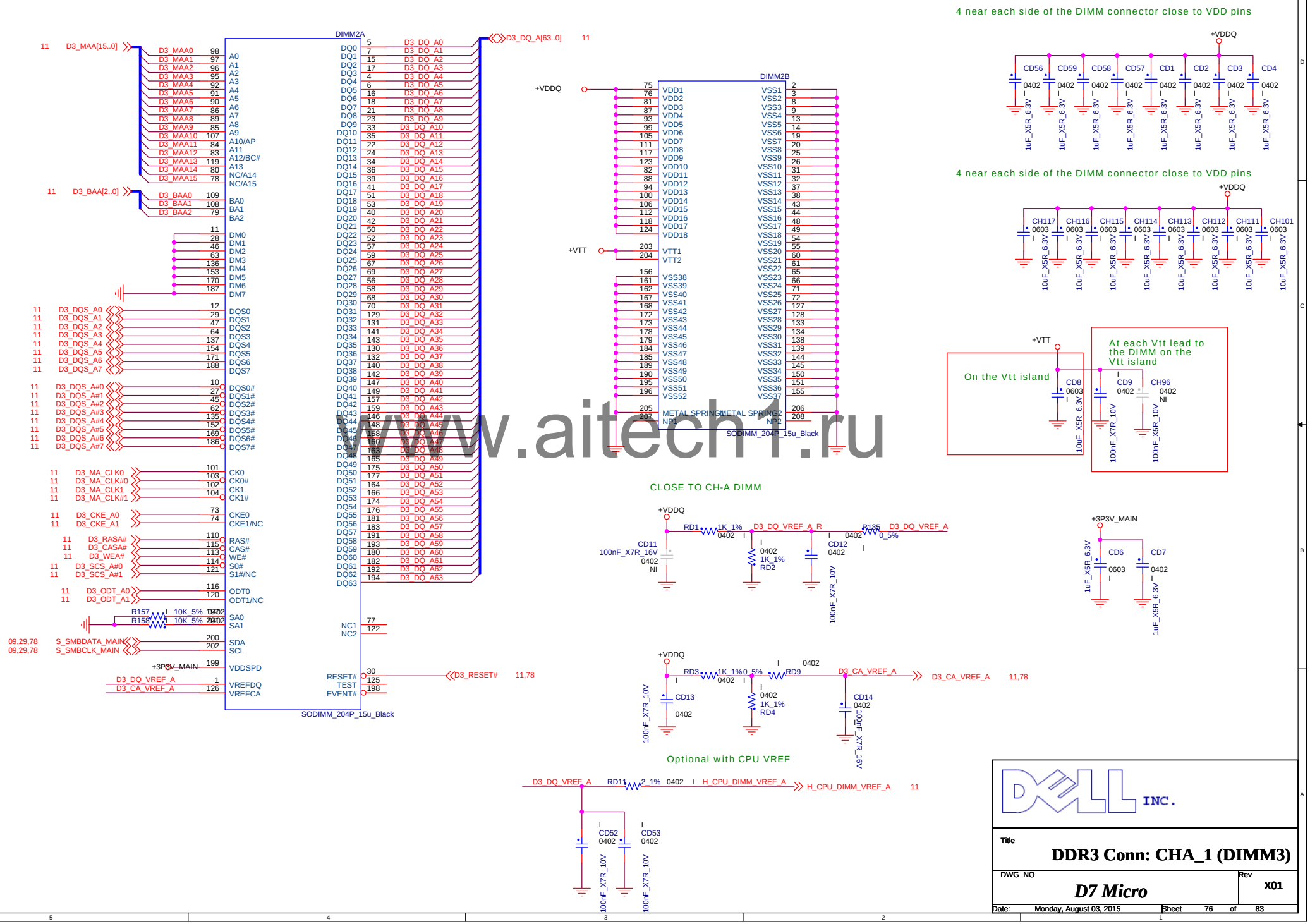
D7 Micro

Rev

X01

Date: Monday, August 03, 2015

CHANNEL A BANK 1
SMB ADDRESS:000



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DELL INC.

Title
DDR3 Conn: CHA_1 (DIMM3)

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D7 Micro

Rev
X01

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DELL INC.

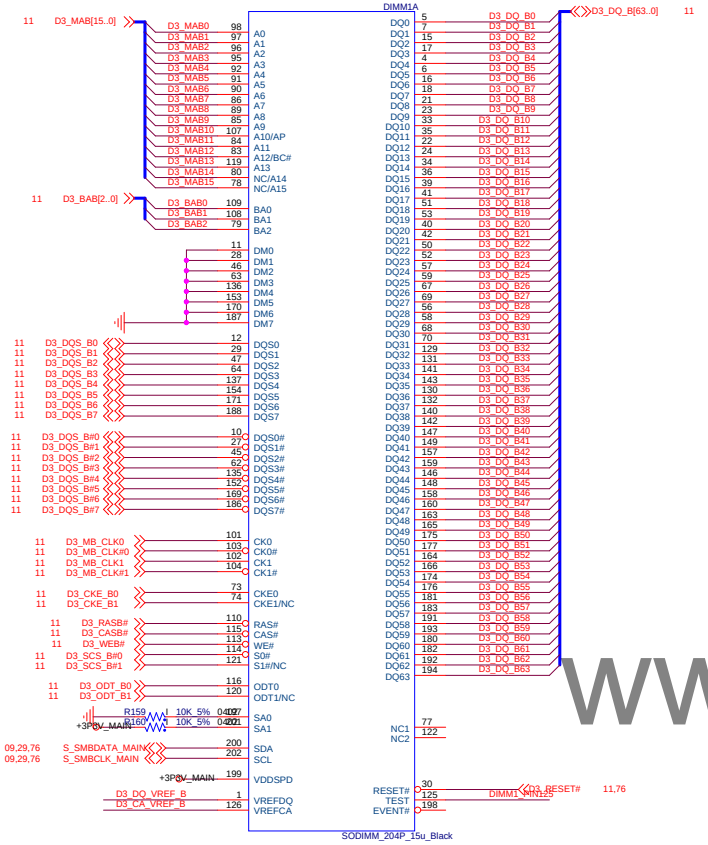
Title: **CPU-1: DDR3_CHA & B**

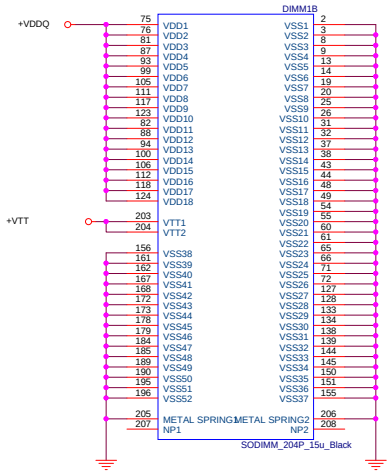
DWG NO: ***D7 Micro***

Rev: **X01**

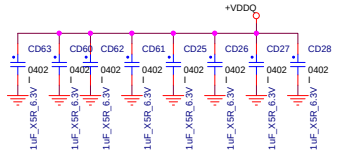
Date: Monday, August 03, 2015

CHANNEL B BANK 1
SMB ADDRESS:010

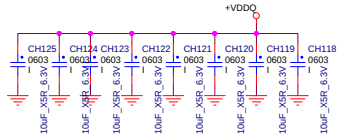


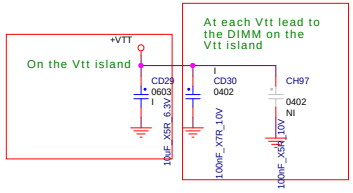


4 near each side of the DIMM connector close to VDD pins

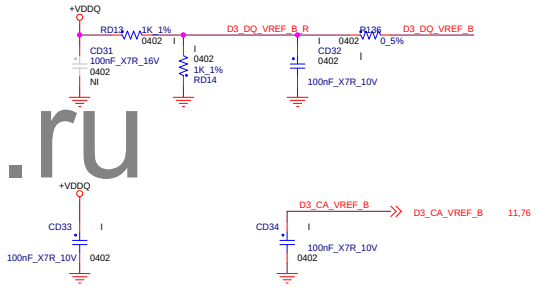


4 near each side of the DIMM connector close to VDD pins

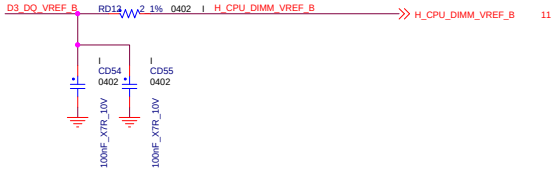




CLOSE TO CH-B DIMM



Optional with CPU VREF



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Title
DDR3 Conn: CHB_1 (DIMM2)

DWG NO
D7 Micro

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Title: **CPU-1: DDR3_CHA & B**

DWG NO: ***D7 Micro***

Rev: **X01**

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DWG NO: ***D7 Micro***

Rev: **X01**

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CPU-1: DDR3_CHA & B

DWG NO

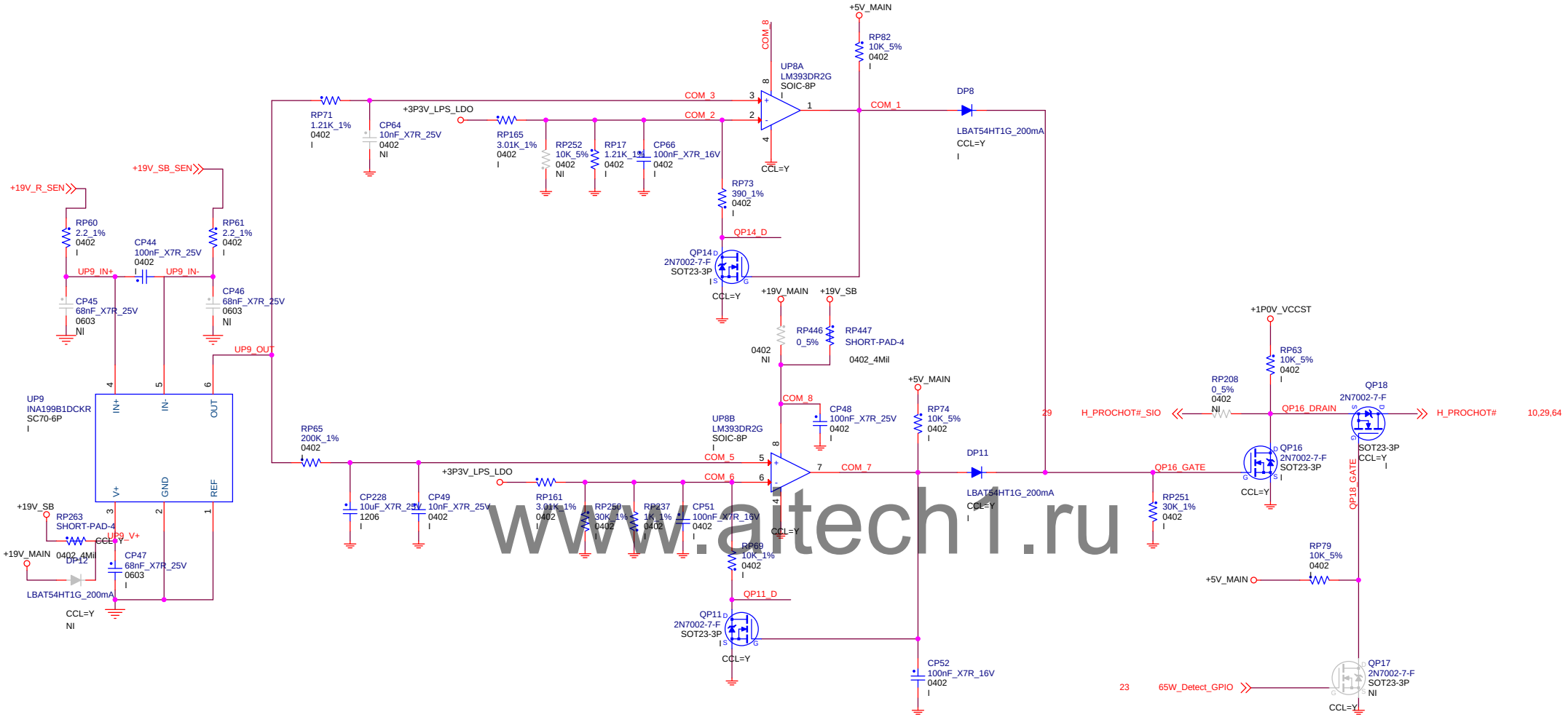
D7 Micro

Rev

X01

Date: Monday, August 03, 2015

65W Detect



65W_Detect_GPIO	MODE
High	For 90W Adapter
Low	For 65W Adapter **Default**

DELL INC.

Title

65W Detect

DWG NO *D7 Micro* Rev **X01**

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2014/05/13 1,change CPU symbal。
2014/05/19 1,X3 update HHPN
2014/05/23 1,Del ECU9 PAGE48
2,change Thermal diode to dip type and Add holder for thermal diode.P40
3,CPU socket change to PE115127-4041-0DH from PE115127-4041-01H follow CT&SFF
4,update power sch follow Morris
2014/05/26 1,change battery and battery holder same as CT&SFF(change back to dogfish)
2,Add RO116,Q2 for NGFF LED
3,RX139 change to 1k form 0ohm
2014/05/28 1,DC pages update (14:00)
2014/05/30 1,Lan Hipot part change.CL21,CL22
2,AUDIO1 part change to 341007B00-24B-H follow Dogfish latest BOM
3,HDD part change to 340712R00-971-H follow Dogfish latest BOM
4,SERVICE_MODE,RTCRST,PSWD part change to 340681Y00-637-H follow Dogfish latest BOM
5,U26 change to 63110ER00-052-H follow Dogfish latest BOM
6,THRM_1,THRM_2 change other vender(FAIRCHILD) because UTC has been forbided
2014/06/03 1,Dummy THRM_3 and THRM_4.Thermal team to quote
2014/06/04 1,update Power solution(DC cost down)
2,remove DP_HDMI(for DP&HDMI option card)
3,update p49---p64(DC 15:00)
2014/06/05 1,update Power solution(P51&63)
2014/06/07 1,Remove OSC(X3--14.318Mhz) of SIO
2,Add R8337,R8338,R8339,R8340(dummy)
3,change R50 to 22.1ohm from 33ohm
4,Remove R6419,R6382,R6422,R6385(PAGE24)
5,Remove R55,R90,R128,R129,R130,R131(P17)
6,Remove PR511,PR518,PR502,PQ502,PQ504,PR503,PQ503,PQ505,PR521,PR504(P63)
7,Dummy EMI Caps(P46)
2014/06/10 1,Realtek Lan change to RTL8111HSD,Add LL2,C110,C111 for RTL8111HSD
2,update DC Part(15:00)
2014/06/11 1,Add CPU Cooler screw hole,MH8,MH9,MH10,MH11
2,update CPU symbol from CIS.Part no change
2014/06/18 1,update THRM_1,THRM_2 HHPN from CIS database
2014/06/23 1,update CPU socket footprint from CIS database
2,Update USB2.0_REAR4,USB2.0_REAR5 HHPN from CIS database
2014/06/24 1,update GPIO A,B,C,D follow D7 SFF table
2,Add R495,R497
3,Remove VGA onboard solution
2014/06/25 1,update GPIO E follow D7 SFF table
2,DP header use 30pin for Dell request,remove 20pin LVDS header from eDP signal
2014/06/26 1,update GPIO F,G,H,I follow D7 SFF table
2,Remove SLP_A schematic
3,Change RO53 to 7.15K,RO54,RO65 to 11K,RO55,RO66 to 0402 page 27
4,Remove R165 page 21
5,R50 change to 33 ohm
6,Remove R137,R138 PAGE10
2014/07/01 1,update DC part
2,change USB power share port follow ARD1.02
3,Remove RO61,RO71,RH3 for cost down---p42
2014/07/02 1,Change USB2.0 CONN for Cost down
2,change TP follow CIS database
2014/07/03 1,Add R375,R376,RX158,RX159 for use chipset SUSCLK for SSD&WLAN,Dummy RX8,RX9
2014/07/04 1,update P58&P60 DC page
2,update VCCIO schemetic
3,Chnage P_VR_READY sequence(P57)
4,Add R377 for WAKE# signal
5,Add R378 for ACPRESENT Pull-H
6,Add PQ943,RP253,RP229 for VTT EN
7,Add U1&U3 for 24Mhz CLK
2014/07/07 1,update UU12 signal name
2,update SSD NGFF slot follow ARD1.03
3,Remove QH2,QH3,QH4 HDMI costdown--P42
2014/07/08 1,update DC part
2014/07/10 1,Use +5VREG swap 5VSB,Delet 5V_S5
2014/07/11 1,Add CPU power2+2 solution
2014/07/12 1,Remove RD18-P08
2,Add R384,
3,Change R139 to 20 ohm from 33ohm,change R140 to 30 ohm from 22 ohm,
change R37 to 30 ohm from 22 ohm,change R48 to 20 ohm from 33 ohm
4,Add 20 pin LVDS Conn for Micro3 VGA module
5,Remove one 1uF CAP for VCCSTG--P12
6,change PI5USB2546ZHEX to PI5USB2546AZHEX
2014/07/14 1,Add R385,RX164,R386,RX165,RX166,R387,R388,R389,R390,R391
2,Remove R324,R323,R325,R60,R61,R327,R326--P20;Remove R365,R277---P21
3,Update RTL8111HSD symbal from CIS
2014/07/15 1,change NGFF to same as dogfish follow ARD1.04
2,Remove R367,R361--p20
3,Remove R360--p21
4,update P51,57,58,59,60,62,64
2014/07/16 1,Check AUDIO schematic follow Demo sch
2,Remove +1P2V_SFROC EN sch
3,DP_HDMI Pin26,30 connect to PCH I2C BU
2014/07/17 1,NGFF SDD config update
2,Remove H110 chipset,SIO 5553,Lan RTL8111,Rear USB2X2.eDP signal,SATA3 signal
3,I,NI to I part(For Micro9):NGFF SSD,RX159,RX1,QX4,Lan 219 part.Rear USB3 part,RP47,
R290,R288,RP42,USB charger part,
4,NI,I to NI part(For Micro3):RP67,QP15,R289,R291
2014/07/18 1,DP_HDMI use new part follow SE request
2014/07/21 1,update DC part(p51,53,54) follow RSV report
2,Remove RV52--P54
3,update DC partP57,58,60,61(1700)
2014/07/22 1,update CPU IML Symbal for layout netin
2,Change LVDS CONN follow SE request
3,Add R396
2014/07/23 1,Remove CO11,RO18 --P26
2014/07/24 1,Change AUDIO1,AUDIO2,DC_IN part follow EMD suggestion
2,update DC part(P57,58,60,61) follow RSV suggestion
3,Add RP34,RP254
4,Remove C160,RS74---p42
5,Update MH10,MH11 footprint follow Dogfish
2014/07/25 1,Remove CA55 --P30
2,Place LU19 part between U66 and USB CONN
3,change RO82,RO78 to 59K,3K(Refer Coral ERP fail)
4,update PU800,PU902,PU701,Y1 from CIS database
2014/07/26 1,Remove RP39,PQ67,RP40,R322,RP38,RP27,RP37,RP44--P50
2,Remove PWR_SWH---p45
3,Add CP229,Dummy ECO1
4,Modify XDP schematic
2014/07/28 1,LAN MDI signal on TVS material pin for Layout
2,Add R398,R399,R400
3,Remove CL11,CL12,CL13,CL14,Dummy CL6---P28
2014/07/29 1,PC955,PC956 link CIS, and the PC955,PC956 EOL. ---P57
2,Modify D4 ---P42
3,Delete PCB ---P35
4,PU601 link CIS ---P57
5,PU701 link CIS ---P61
6,PU800,PU902 link CIS ---P55 and P62
7,Dummy QV12,QV13. ---P42
8,Modify CA89 source. ---P30
9,Modify C145 source. ---P22
2014/07/30 1,Modify R57,QX2,QX5,PQ2 main source. ---RDE make BOM
2,Modify QH1,QH5 main source. ---RDE make BOM
3,Modify C8,C123,C124,C138,C141,C142,C143,C149 source ---RDE make BOM
4,Delete FB5,FB6,FB7,FB8 ---P34
5,Modify PC955,PC956 main source. ---P57
2014/07/31 1,Update DC Page70
2,Change net name TP_APU_RSVD_AV39 to TP_APU_RSVD_B39
3,Change net name TP_APU_RSVD_AW38 to TP_APU_RSVD_J17
4,Delete 1.8V power: P1V8_P3V3_PCH_GPPA. ----62
5,Update MH7,MH6,MH5,MH3,MH4,MH2,MH1 footprint. ---54
2014/08/01 1,Delete MH8,MH9,MH10,MH11 GND. ---P10
2,Modify DP7,D3,DP1, QV12,QV13,QH1,QF1,QH5,QL3,QP6,QP9,QP44,QP11,QP14,QP17,
QP18,QP16,PQ2,QP27,QP31,QP36,QA40,QA41 source, change NXP source.
3,Modify Y1 source. ---P25
4,Modify THRM_1,THRM_2 source. ---P50
5,Add PCB. ---P46
6,Modify DA2,DA3,DA12 sourec. ---P35
2014/08/02 1,USB2.0 signal ESD UU8,UU9,UU16,UU12 dummy.
2,Change RF24 from NI to PROTO.
3,Delete power O_SUS_5VON. ---P61
2014/08/04 1,Modify Power Net, follow SFF power net name.
2,Change SPI1,PCE611,PCE612,PCE613,PCE614,PCE615,PCE621,PCE622,PCE948,PCE949,
PCE601,PCE602,PCE625,PCE950 source.
3,Change CD8,CD29,CX16,PC650 source. RDE make BOM.
4,Dummy RO11. ---P29

2014/08/05 1,Modify Gasket1,Gasket2 Mfg name.
2,Change D4 source. ---P39
3,Update SIO and PCH GPIO.
2014/08/06 1,Modify DC_IN source. ---P60
2,Add MOS. ---P65
3,Modify USB OC Port.
2014/08/07 1,Modify UH1 pin H1/H2/H3. ---P10
2,Modify Silkscreen.
2014/08/08 1,Delete P54 EMI Cap. ----P54
2014/08/09 1,PCH HeatSink U4_1 add one Pin. ---P26
2014/08/11 1,Modify CL21/CL22 source. chang to BS401N. ---P33
2,Update all Power Page. From Page59 to 82.
3,Add CX80,CX81,CX82, for EMI. ---P13
4,Change DA2,DA3,DA12 connect A_GND to GND. ---P35
5,Delete PR247,PC245,PR250,PR965,PR249,PQ108 ---P67.
6,Follow Intel's suggestion: ---P23,24
GPP_G0~GPPG23 pull up power rail change to AUX power (VGA_Cable_Detect, Config_0
pull up power change);
GPP_G6 change to GPP_H3.
2014/08/12 1,Delete CX80,CX81,CX82 ---P13
2,Modify USB2.0 signal name (Common choke to connector) ---P43
2014/08/13 1,Change DA2 pin order ---P13
2,Modify DC part.
2014/08/14 1,R351 change to NI. USB charging IC no need Pull up ---P23
2,GPP_H3 change to GPP_G6, keep +3P3V_MAIN power rail.Follow Wistron's Design.---P23,24
3,RF41,RF42 change to 15 ohm. Follow PDG ---P51
4,Change PCB description. ---P46
5,R123 change to 8.2k ohm. Follow CRB. ----P23
6,Modify QO1,QO2,QO3,QO5,QO20 source. ---P30
7,RL87 install. Intel's suggestion. ---P31
8,PCIE_100M_7_N connect to CLK Pin E5,
PCIE_100M_7_P connect to CLK Pin G4,
PCIE_100M_1_N connect to CLK Pin D5,
PCIE_100M_1_P connect to CLK Pin E6. ---P25,57.
2014/08/14 1,PCIE_CLKREQ1 change name to PCIE_CLKREQ9. ---P24
2,PCIE_CLKREQ9 connect to Pin BC32 (REQ9). ---P24
3,PCIE_100M_1_N change name to PCIE_100M_9_N. ---P25,57
PCIE_100M_1_P change name to PCIE_100M_9_P. ---P25,57
4,PCIE_100M_9_N connect to CLK Pin N3,
PCIE_100M_9_P connect to CLK Pin N9. ---P25
5,Delete TPS85,TPS86. ---P25
6,Add R6590 and R6591. Follow CRB ---P24
7,Add CA102, CA103, CA104 NI and CA105 NI. Vendor's suggestion. ---P34
2014/08/15 8,Delete RF45. ---P45.
9,Add RF43. ---P45
10,Delete RF63. ---P45
11,TPM_P14_NCT_VDD pull high power change from +3P3V_MAIN to F_SPI_VCC.
and add RF54 pull up +3P3V_MAIN. ---P45
12,Update Power part.
13,Reserve RF54,RF63 pull power +3P3V_MAIN. ----P45
14,Add RF68. ---P45
15,Modify THRM_1,THRM_2 source. ---P50
16,MOdify PCE42,CP199,ECO1,CP198,CP196 source.
17,Delete R308,R309 to A_GND. ---P35
18,Modify Sponge1 source to 7D080U600-JES-H. ---P46
19,Modify TPM Pin8,14,22 power name and CAP. ---P45
20,Modify DIMM1.DIMM2 source.
2014/08/18 1,Update Power part.(20140815-1740)
2,Reserved RA32,RA37. ---P34
3,Dummy CA103,CA102. Change CA1,CA2 to 22uf. ---P34
2014/08/19 1,Delete R308,R309. ---P35
2,Add Pull high R85(NI). ---P10
3,Add connect to GND through 470pF(CO50) cap(NI) ---P55
4,Install RO11. ---P29
5,Pull up to +3P3V_AUX through RO106(8.2K Ohm) resistor. ---P29
6,Change SMBUS S_SMBCLK_RESUME/S_SMBDATA_RESUME connect to CPU_XDP. ---P9
7,Change R52 to 1K ohm(NI) -----P10
8,R84 change to 20K ohm. ----P25
9,Power Part update.
(1)add 0 ohms for co-layout VCCIO and VCCSA power rail.
(2)add PL953 for VCCSA_IN.
(3)change PR233&PR174 100 Ohm to 10 Ohm.
10,Power Part update.
(1)add 0 ohms for co-layout VCCIO and VCCSA power rail,change PR174
to 10 Ohm--page68
(2)add PL953 --page67
(3)add PC60,PR61,PR93;change PR613,PR662 connection;PR610 NI-I. --page64
11,Change RO53,RO54,RO65 to 9.1K ohm. Change RO66 to 6.8K ohm. ----P30
12,Change R62 to 0 ohm. ---P22
13,Move CA103 to arrow position and connect to DGND. --P34
14,Change QA41 S pin to AGND. ---P35
2014/08/20 1,Update Power part.(20140820)
2014/08/21 1,Modify THRM_1,THRM_2,INTRUDER,ECL1,CH79,CH80 source. ---P50
2,Add CA106 to AGND ---P34
3,LPC RST change to SIO PIN52, and renamed to S_PLTRST_LPC#.
And add RO104(NI) pull high +3P3V_AUX ---P29
4,U27and U28 Pin5 connect to +3V_LAN. ---P33
5,CU20 change from 100nf to 10uf. R316 change from 20K ohm to 82K ohm. --56
6,USB_CHARGING change to PI5USB2546ZHEX. ----P56
7,RL20 NI. ---P31
8,Add CL60,CL61,CL62,CL63,CL64 and CL65. SFF Intel's suggestion ---P33
9,R282 change to 49.9k ohm. R173 change to 4.7K ohm. SFF Follow CRB ---P24
10,Add RF69(NI) pull high to F_SPI_VCC. ---P45
11,Add RF70(NI) connect TPM_SERIRQ and F_SERIRQ#. ---P45
12,DA3 change pin order. --P34
13,Delete CP229, change ECO1 from NI to I. ---P46
14,Modify R396 pull down connect to SIO Pin19. ---P24,29
15,Add CO51 pull down connect to O_Yellow#. ---P55
2014/08/22 1,Change RL20 from NI to I. Intel review SFF ---P31
2,Modify UU8,UU9,UU12,UU16 source. ---P43/56
3,Add RP44 SFF Intel's suggestion---P26
4,Pin20 connect to +3P3V_SB SFF Vendor's suggestion. P34
5,RSVD[18] H8,RSVD[11] K12,RSVD[8] L12 connect to TP, not connect GND. SFFIntel's suggestion. P10
6,Delete R151 to GND,and RSVD[10] K13 connect to TP. ----P10
7,Add RX167(NI) circuit ---P57
8,Delete RL5 circuit. ---P31
9,Add R6543 pull high. This is needed to reduce leakage from Coin
Cell Battery in G3 state. ---P24
10,Add UEFI TP. --- P23
11,Update DC part. P64:DEL PR660, P67:DEL PR229,ADD PR228
12,Delete RD18. ---P11
13,Modify CH79,CH80 source,change value. P11
14,Power update, Del:CP67 , CP231 Page 61
15,Add RP62,RP67,QP15. ---P29
16,DIMM2,DIMM1 link CIS. ---P76,78
2014/08/25 1,Modify Y5 source. CE suggestion.
2,Add RP64.And modify Q13 circuit. ---P29
3,Dummy RO113, RO114, QO20A, QO20B, RO115. ---P30
4,PR406 pull high power change to +5V_AUX. ---P56
5,DDR_VTT_CNTL add testpoint TPS54. ---P11
6,R133,R134 change to Short pad. ---P11
7,R79 power rail change to 1P0V_PCH_VCCF24_FB_R. SFF Intel's suggestion ---P25
8,Delete R6543 pull high. S_INTRUDER# already have pull up. ---P24
9,PCH_USB2_OC7 change to PCH_USB2_C2. --P24
10,Add QX6, and modify QX6(NI) circuit. --P57
11,Remove CL60, CL61, CL62, CL63, CL64, CL65. LAN reference GND ---P33
2014/08/26 1,update DC Page65,66.
2,Delete signal Memory Detect_CTL. ---P23
3,Modify AUDIO1,AUDIO2,DC_IN,KB_MS_SERIAL source. ---P35
4,Add C158 to GND. ---P26
5,Modify THRM_1,THRM_2,Sponge1 source. ---P50
6,Modify PCE601,PCE602,PCE952 source to PANASONIC 25SVPF47M. P65,70
7,Change RP64 from NI to I. ---P29
8,Modify R298 from 10 K to 100K ohm. ---P29
2014/08/27 1,P62-modify PU901 pin3 connection.
P68-del PR360.
2,Modify GPIO S_SER2_DE2T# from GPP_F9 to GPP_B4. ---P23,24
3,Delete Q1,R253,R248 circuit. ---P14
4,RH66 change to PROTO, R150 change to 1K ohm I. ---P10
5,Delete R144 pull high. ---P10
6,Change RH51,RH65 value, and delete RH47 pull VCCIO. --P9
7,Add C74,R91 circuit.Modify RH73 value,change NI to PROTO. ---P9
8,Add R14. ---P10
9,Delete CS71,R172. --P9
10,Add RS15.Delete RH75. Delete RS249. --P52
11,Delete R233 pull high.Modify R232 value. ---P26
12,Add C75,R151,C70. ---P9
13,Modify R170. ---P24
14,Add RP5.Delete R64 pull high. ---P22
15,Delete U1,CF25 --P45
16,Delete U3,CF26 ---P53
17,Modify R139 value. P22
18,Delete TPS32, add R55. --P10
19,Modify RS159 pull high power from +3P3V_SB to +3P3V_AUX. ---P28
20,R6334 change to R402;R6335 change to R403;R6590 change to R404;R6591 change to R405;
21,Modify QV3,QV4,QV5,QV6 circuit. ---P40
Add Q15,Q16.
22,modify PC706 ,NI PC708 -P67
modify PR217,PR218, -P70
modify RP256, -P72
add PR289 -P62
23,Modify PC973,PC978,PC800,PC809 source to MURATA_ GRM31CR71E106KA12L. P68,69

2014/08/28 1,Delete TPS79,add R106 to GND. ---P14
2,Add R108,R113 to GND. --P14
3,Net name N18927879 change to GPP_B12_SLP_S0_N. P24
4,Net name N23246667 change to PU17_PGOOD. ---P72
5,Net name N16799268 change to VCCPLL_OC_AJ9. ---P14
6,PCIE_100M_9_N/PCIE_100M_9_P change to PCIE_100M_5_N/PCIE_100M_5_P. ---P25,57
7,Delete D3,QV12,QV13; Add UV7 ESD. ---P39
8,PCIE_CLKREQ9 change to PCIE_CLKREQ5. ---P25,57
2014/08/29 1,Modify UV7 source to ON/ ESD7004MUTAG. ---P39
2,Add UU16 pin1,pin6 testpoint. ---P43
3,U66 add net U66_STATUS# for testpoint. ---P56
4,UU8 add net UU8_PIN3,UU8_PIN4 for testpoint. ---P43
5,Modify DC part:
(1).modify PR256 P72
(2).modify QP20 P61
(3).modify PR151 P67
6,CL7,CL8 change to 22pF. ---P31
7,CL84 change to 1uf. ---P33
8,U_USB11N,U_USB11P change to U_USB9N,U_USB9P. ---P21,57
9,SPI1 change name to @SPI_1. Fellow RDE suggest. ---P51
10,Modify DC part:
(1)modify PR151,PCE701,PCE951 P67
(2)modify PCE611-615 P65
(3)modify PCEP948,PCE949,PCE621,PCE622 P66
PC945-PCE945 P70
(4)modify BOM CCL ISSUE
11,Modify DP connector source. ---P40
12,Delete C112. ---P14
13,ECO1 change to 220uF. ---P46
14,R351 stuff. ---P23
15,RH2,R91 change to 2.2K ohm. --P9
16,Add FAN OFF control circuit; FAN pin2 change power rail.
Add CPU_FAN_OFF connect to GPP_G19. ---P23
17,XDP_CPU Pin 51 and Pin 53 connect to S_SMBDATA_MAIN and S_SMBCLK_MAIN. ---P9
18,XDP_CPU Pin 55 connect to XDP_PCH F_PCH_JTAG_TCK_FILTER. ---P9
19,Modify DC Part:
(1),modify QP13 ,add PR9
(2),modify QP26,CP232,
(3).modify LP14,LP15
2014/09/01 1,Modify ECO1 power to CPU_FAN_+5V. ---P46
2,Modify RH63 to PROTO. ---P10
3,Modify RP5 to NI. ---P22
4,Add CS83,RS2,RS169; and modify RS253 to 0 ohm. ---P52
5,RH63,RH66,R32 change to NI. Add R18. ---P9
6,Remove RP5. ---P22
7,Add RH75,RH76,RH77. ---P9
8,R150 modify to 51 ohm. ---P10
9,Add C2 to GND. ---P46
10,USB CHARGING circuit follow Wistron.Modify charging PIN4,6,7,8. ----P56
11,R32 change power to +1P0V_PCH_AUX. ---P9
12,Add R177,R178,R179. ---P9
13,modify PQ13 and PQ20. ---P61
2014/09/02 1,Modify FBA5,FBA7,FBA9,FBA8 SOURCE. ---P34
2,Modify FV1 SOURCE. ---P40
3,Modify DC part: PC702 - P67,
PC172,PC169 - P70,
PC191 -P72
4,Modify R108,R106,R113,R112 source,change to 0603. ---P14
5,Add SLOT3_M.2 colay with SLOT2_M.2. ---P57
2014/09/03 1,Modify FBA6 SOURCE,change to HCB2012KF-800T30. ---P34
2,Modify QF3 source, change to AP2303GN. ---P46
3,Add C3 to GND. ---P46,
4,Modify DC part:modify PC651,PC653,PC654 color - P65,
PC969,PC642,PC970,PC662 - P65,
PC971,PC682,PC998,PC1005 -P66.
RP151 -P67
PR217,PR218 -P70,
RP256 - P72,
2014/09/03 1,Modify FBA7 source, only for IR Drop. ---P34
2,Modify DC part:
(1).Add PR361,QP76 for deep sleep sequence.-P59
(2).Add PQ77 for Mosfet derating. - P61
3,Modify DP connector source,change back to FOXCONN_3VD11207-87AA-4H. ---P40
4,Config_0 change to PCH Pin N42. ---P23
5,Add testpoint FVS_TP to PCH Pin L43. ---P23
6,Modify DC part
modify PC903 -P62
modify part property.
7,Modify FVS,UEFI testpoint. ---P23
8,Modify rear USB port. ---P43
9,Modify FVS,UEFI footprint. ---P23
10,Modify R236,R237 source. ----P26
2014/09/19 1,Change QL7 to AP2303GN-HF. ---P32
2014/09/22 1. Change NGFF key B slot to key M and its peripheral circuit.--P57
2. Add +3P3V_PCIAUX1 power circuit.--P61
3. Change RX155/RX156/RX167/RX154/QX1/QX3/RX153 BOM option from I to PROTO.--P57
4. Change QF1,QH1,QH5,PQ2,QP6,QP11,QP14,QP16,QP18,QP27,QP31,QP44 from 2N7002LT1G
to 2N7002-7-F.
5. Updating +3P3V_PCIAUX power control circuit.--P29&P23

2014/09/24
1. Adding DP portD lane[1:0] and DDPD control signals --P41
2. Changing eDP[3:2] to DP portD[3:2]. --P13
3. Adding USB1N/1P net into SSUSB1_F. --P56

2014/10/06
1. Swap pin1 and pin2 for UU14. --P43
2. Add R308 to connect GND and add net "V_DDSP_D_HPD" to connect pin AV4--P23
3. Change PC903 PN to 620109N01-015-H from 620109N02-015-H. --P62
4. Change U139 footprint to VTQFP_128_16_630 from TQFP128B. --P29

2014/10/07
1. Change "S_WAKE#" net to U4.BD11 from U4.BC13. --P24

2014/10/08
1. Change RH73 BOM option from PROTO to NI. --P9
2. Change R32 BOM option from NI to I. --P9
3. Change R347/R348/R355 BOM option from NI to I. --P23
4. PSWD_JUMPER(1-2) rename to PWCLR_JUMPER(1-2) --P28
5. R50 change to 20 ohm; R6 change to 100 ohm--P10
6. Reserving RO118--P29
7. Adding RP46 pull up to +3P3V_AUX, change R226 to NI from I.--P26
8. Adding R6608 on H_PWRGOOD connect to PCH.--P10
9. Changing R392/R393 power source to +3P3V_AUX .--P22
10. Stuffing R174 and adding C1743(1uF) .--P24
11. Stuffing RH66 and RH63 .--P10
12. Changing C289/C290/C291/C292 to BS4200N-C from BS401N .--P33
13. Changing XL1 from DIP to SMD .--P32

2014/10/09
1. Remove RX174/RX166. --P57
2. Remove R386/R387. --P22
3. R32 and R397 PU change to +1P0V_VCCST. --P09
4. R249 unstuffed.--P14
5. Replace DC circuit from P59 to P82.
6. Change config_1 to U4.AR31, remove R369, change C1743 to C18.--P24

2014/10/10
1. Change QF2/QF7 to 2N7002-7-F from FDV301N --P46
2. Stuff R401. --P23
3. Change PCH_WAKE# to S_WAKE#. --P23/57
4. Updating PCB information --P46
5. Updating M2 slot to 34031A200-600-H from 34031DD00-600-H for ME request. --P57
6. Change FU6/FU7 to SMD0805 from SMD1206 and change SSUSB3_R power to USBPWR4_F_50,
SSUSB1_R power to USBPWR2_F_50. --P57
7. Change overall DC circuit. --P59~P82
8. Change RH59 pull high to +1P0V_VCCST.--P9
9. Adding C160 to GND.--P33
10. Adding RX174/RX166/R88 for M2_WAKE# .--P23/P52/P57
11. Adding SLP_WLAN_N net.--P24
12. Adding RO119/QV72.--P29
13. Swap pin R41 and pin P43.--P23

2014/10/10
1. Change U26 footprint to TP_25_39.--P33
2. Change RL12 to RL15 sync up with Micro7.--P32
3. Change CL36&CL35 to CL7&CL8 sync up with Micro7.--P32

2014/10/10--D7-MICRO3_B00_A_SCH_1011_2014_1425
1. Change PCH_XDP circuit sync up with Micro7.--P52
2. Remove R342/R343 sync up with Micro7.--P23
3. Change R364 to RU1 sync up with Micro7.--P23
4. Adding CP229 sync up with Micro7.--P46
5. Adding R28/R29 sync up with Micro7.--P24
6. Adding RF44 sync up with Micro7.--P53
7. Adding RV17/RV18 sync up with Micro7.--P41
8. Changing FU10 to 2A sync up with Micro7.--P56
9. Changing QA40/QA41/QL3 to 2N7002-7-F from 2N7002LT1G sync up with Micro7.--P35/P33
10. Changing LAN_WAKE# to L_LAN_WAKE_N sync up with Micro7.--P24/P32

2014/10/13--D7-MICRO3_B00_A_SCH_1013_2014_0800
1. Change M2.key M circuit sync up with Micro7.--P57

2014/10/13--D7-MICRO3_B00_A_SCH_1013_2014_0900
1. CL29,CL30 change to 10nF; Remove RU86,RU87, add CL60 and CL61.--P57

2014/10/13--D7-MICRO3_B00_A_SCH_1013_2014_1440
1. Change ECO1 footprint.--P46
2. Change DC overall circuit.--P59~P82

2014/10/13--D7-MICRO3_B00_A_SCH_1013_2014_1730
1.Delete SIO_PIN110,SIO_PIN76, ---P29
2.Delete PR213_PIN2, ---P70
3.Delete PU612_PIN2,PU904_PIN2 ---P66
4.Delete PR158_PIN2 ---P72
5.Add DIMM1_PIN125 ---P78
6. Change DC overall circuit.--P59~P82
7. Stuff UU8,UU9,UU12,UU16 for ESD test failure issue.--P56/P43

2014/10/13--D7-MICRO3_B00_A_SCH_1013_2014_2015
1. Delete CP229, stuff ECO1.--P46

2014/10/14--D7-MICRO3_B00_A_SCH_1014_2014_1008
1. Stuff RL34.--P32
2. Change FU10 to 2.6A from 2A.--P56
3. Add R408,R409,R410.--P59/P24
4. Add R115 connect to P_VR_READY. --P9
5. SIO PECI Pin 29 and 31 power rail change to +1P0V_VCCST. --P29

2014/10/14--D7-MICRO3_B00_A_SCH_1014_2014_1410
1. Change PETS to APS/PETS .--P53

2014/10/14--D7-MICRO3_B00_A_SCH_1014_2014_1900
1. Change CO23 power well to +1P0V_VCCST .--P29
2. Change @SPI_1 from MICRON to MXIC .--P51

2014/10/15--D7-MICRO3_B00_A_SCH_1015_2014_1000
1. Adding R87.--P24
2. Adding NC pin net(PR213.2,PR158.2,CPU.AT16,CPU.AL25,CPU.AM25,CPU.AL26,CPU.AM26,
CPU.AP20,CPU.AP15,CPU.AM15,CPU.AL15,CPU.AU12,CPU.AV10,CPU.J2,CPU.J1,U4.A39,U4.B38,
U4.P1,U6.84
1, SLOT1_M.2---pin: 17, 19, 21, 23, 25, 27, 6, 48;
2, XDP_PCH----pin: 48, 53, 5,
U6.110
U4.R2).
3. Changing UU16/UU12/UU8/UU9 from AZC199-04S to AZC199-04S.R7G.--P43/P56
4. Changing DC overall circuit.--P59~P82

2014/10/15--D7-MICRO3_B00_A_SCH_1015_2014_1420
1. Adding R92.--P24

2014/10/15--D7-MICRO3_B00_A_SCH_1015_2014_1730
1. Add C5,R19,PU21 circuit.--P24

2014/10/17--D7-MICRO3_B00_A_SCH_1017_2014_0850-Q170 for B00 BOM
1. Changing C289,C290,C291,C292 P/N to 520600R00-52N-H from 520600R00-52N-G--P33
2. Changing audio codec mfg P/N to ALC3234-CGT from ALC3234-CG--P34
3. Changing component side. --all
4. Changing overall DC circuit. --P59~P82

X00 change list

2014/12/15--D7-MICRO3_X00_SCH_1215_2014_1400
1. Delete RD10,RD15,RD16 for Vref_CA part ---P78
2. Changing the USB2.0 CONN , SSUSB3_R, SSUSB4_R to FOXCONN/UBA1117-14151-4F from
FOXCONN/UB1112C-4K5-4F for plating change from 30u to 15u -- P43
3. Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1212_2014_DC-DC DDR3.DSN
4. Changing PCB1 description to Red soldermask and white silkscreen Ver:X00 ,
PN to 0101AYH02-491-G-- P46
5. Changing SKU ID to Micro3: dummy R354, install R352,
Board ID to Ver:X00, dummy R290, install R291 -- P28

2014/12/20--D7-MICRO3_X00_SCH_1220_2014_0930
1. Change R from 2.2ohm to 2ohm by new PDG RD17,RD11,RD12 ---P11,P76,P78
2, Change value of RO108 , RO109, C2 from 2M OHM,10OHM,1nF to 47K OHM , 100K OHM ,
100nF ----p46
3, Change ECO1, CD14 HH PN . ---P46,P76
4, remove R121 and R388 change the GPIO from GPP_F21 to GPP_G11 for Wifi disable2 --P23
5, add R431.R432, use GPD0 for usb smart power control in DSW -- P23,P24
6, change QO22B PIN C net from OQ14_C to O_FIO_SATA_LED# for SSD led issue -- P57
7, Wlan clk from port 5 to port 0 , and change the net name -- P25.P57
8, Wlan REQ from port 5 to port 0 , and change the net name-- P24.P57
9, Change the Pull up power, R383,R273 connect to 3.3V AUX-- P24.P57
10, dummy RX17,RX153,RX154,RX175,RX155,RX156,STUFF RX158,RX140 -- P57
11, dummy R389 as pull up duplicate , -- P24
12, change ref PWRGD to PWCLR -- P28
13, dummy RX12,RX14 -- P57
14, Remove R380,R123,RF67,RF62,RF46, RF58,RF49,RF47 circuit for remove the LPC I/F
of TPM. -- P23,P45
15, delete net FM_LPC_CLKRUN# , remove RF64, RF43, RF65, RF54, RF63, RF70 -- P23,P45

Above change is base on D7 Micro7 T00

2014/12/20--D7-MICRO3_X00_SCH_1220_2014_1530
1. remove R264 . Change R300 from NI to I by follow SFF ---P23,P29
2, dummy RL85 , RL86 , -- P22
3, remove R328 ,R329,R403,R402,R278,R373 -- P22,P24
4, Change UX3,UX2,UX4 PIN 5 from +3.3V_MAIN to +3P3V_PCIAUX by follow SFF -- P57
5, change MBR0540T1G to B0540W-7-F;
Change ESD7004MUTAG to AOZ8809DI-05 ;
change MMBT3904LT1G to MMBT3904-7-F;
change 2N7002DW-7-F to 2N7002DWA-7-F;
change SN74LVC1G17DCKR to 74LVC1G17SE-7
by follow SFF -- P57,P24,P29,P39,P40,P41,P43,P32,P33
6. change the power of R203, from 3.3V_main to 3.3V_aux by follow SFF ---P26
7. Dummy RX13,RX26,QX2,UX1,CX16,QX5,RX167,QX1,QX3 by request ---P57
8, Dummy R391, add R435,and PU to +3P3V_PCIAUX1 -- P57,P24
9, change RV24,RV25,RV27,RV28,RV29,RV30,RV36 package from 0402 to 0603 for DFM -- P40

2014/12/22--D7-MICRO3_X00_SCH_1222_2014_0930
1. change RP84 connection from S_SLP_S4# to S_SLP_S3# ---P29
2, Skylake-S Ball H8 change from RSVD to VSS -- P14
3, change R19 from 0 ohm to 22 ohm for fine tune waveform -- P24
4, add R436 ,R437,R438,R439 for fine tune waveform -- P24,P23
5, change the value of RO52 from 8.2K ohm to 10K ohm -- P30
6, update CONN's plating , audio1 HH PN, -- P35
HDMI HH PN , -- P35
SSUSB2_F , SSUSB1_F, -- P56
SSUSB2_R, SSUSB1_R -- P43
7, Change the PN of HDD_LED -- P55
8, Change the DP_VGA CONN's PIN 26,30 connect to S_SMBCLK_MAIN,S_SMBDATA_MAIN -- P41
9, remove R392 , R393 for no usage of I2C0 -- P22
10, change CA12 from NI to I, and change the value of CA12 from 22pF to 4.7 pF -- P34

2014/12/22--D7-MICRO3_X00_SCH_1222_2014_1200
1, Change C3 from I to NI -- P46
2, Change R255 POWER +5VAUX_LPS_LDO TO +5V_AUX for ERP -- P53
3, Change C272 C275 from 4.7uF to 10uF -- P35
4, QF3 HHPN from AP2303GN-HF to AO3409L -- P46
5. Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1218_2014_DC-DC DDR3.DSN

2014/12/23--D7-MICRO3_X00_SCH_1223_2014_1130
1. add R0120.RO121, and pull up to 3.3V AUX ----P29
2. Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1223_2014_DC-DC DDR3.DSN
3. change RP84,RP85,RP70,Q18 from I to PROTO as the M2 slot is not PRD --P29

2014/12/24--D7-MICRO3_X00_SCH_1224_2014_1130
1. add usb charger for option ----P56
add GPIO -- GPP-G15, GPP-G16 -- P23
add GPIO -- GPP-H0, GPP-H6 -- P24
add OC6# -- P23
2014/12/24--D7-MICRO3_X00_SCH_1224_2014_1530
1. add C322,C323,C324,C325 for usb eye diagram -- P43,P56

2014/12/26--D7-MICRO3_X00_SCH_1226_2014_0930
1. change Location from SPI_1 to SPI ,from @SPI_1 to SPI_1 --P51
change Location from @U26 to U26_1 --P33
2, change the Gasket from FEIMA_2J0533800-52R-H to SPEEDGOLD_DSG547,
from FEIMA_2J0535N00-52R-H CE to SPEEDGOLD_DSG548 -- P46
3. change QL7 from AP2303GN-HF to AO3409L for BOM/DFM -- P32

2014/12/29--D7-MICRO3_X00_SCH_1229_2014_1200
1, Dummy the RF35 -- P53
2, change MFG PN of the location HDD from C166LH-122ZC-Y to LD2722V-SUML1H -- P42
3, change some component CCL=Y
4, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1229_2014_DC-DC DDR3.DSN
2014/12/29--D7-MICRO3_X00_SCH_1229_2014_1715
1, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1229_2014_DC-DC DDR3_1700.DSN
change PCE701,PCE951
2015/01/04--D7-MICRO3_X00_SCH_0104_2015_0930
1, correct the SATA LED connect -- P57
2, change RU122, from 0603 to 0402 --P56
3, change the CF20 connect for layout --P45
4, updated the HDD_LED P/N --P55
5, change MH8,9 MH10,11 footprint to MH_182_280_D7MICRO, MH_170_280_D7MICRO --P10
6, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_1231_2014_DC-DC DDR3 .DSN

2015/01/04--D7-MICRO3_X00_SCH_0104_2015_1400
1,Add dummy res R440 and pull up to 3P3V_AUX --P10
2.Add dummy res RU129 and pull up to 3P3V_AUX ---P56
3,Change the Value of C116 and C117 from 15pF to 18pFN --P25

2015/01/05--D7-MICRO3_X00_SCH_0105_2015_0930
1, link CIS for some component
2, del the net of pin10 of UF1 -- P45

2015/01/07--D7-MICRO3_X00_SCH_0107_2015_1130
1, Change the Value of R124 from 22 Ohm to 15 Ohm---P23
2, del the C322,C323,C324,C325 for BIOS solutioin of usb eye diagram -- P45
3, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_0106_2015_DC-DC DDR3 .DSN

2015/01/07--D7-MICRO3_X00_SCH_0107_2015_1700
1, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_B_SCH_0107_2015_DC-DC DDR3 .DSN

2015/01/10--D7-MICRO3_X00_SCH_0110_2015_1400
1, RO52 DDR4 use 10k, DDR3 use 8.2k -- P30
2. Change KB_MS_SERIAL pin define ,swap PIN 13/ PIN 24 , PIN13 to GND , pin24 to detect
change the DP-VGA pin define, pin20 to SMB_DATA,pin21 to GND,
pin29 to VGA detect, pin30 to DP detect-- P41
2015/01/13--D7-MICRO3_X00_SCH_0113_2015_1930
1, change PCB CCL from Y to N -- P46
2, add 0.1uF NI cap CV53 for internal SPK detect pin --P35
3, Add C322,C323,C324,C325 ,C326,C327,C328, C329,C330,C321 for co-lay with usb power ecap -- P45,P56
4, change the MFG PN of CA88 , from GRM21BR60J225K to GRM21BR60J225KA01L -- P34
5, add NI RO122 and NI RP445 for PCIAUX_GATE1 -- P29
6, change CH3 from I to NI for D3_Reset -- P11
7, Swap QF3 PIN D and PIN S for cpu fan power -- P46
8, remove R440 for remove the cpu_select pull up -- P10
9, Change PCH MFG PN. from 943313 to 940717 QHPT for new version chip -- P21-28
10, add Q20,Q19,RO129,RO127,RV54,RF70,RO126 for diag led when cpu uninstall -- P29
11, change SLOT_M2 FOOTPRINT to NGFF_75_20_862X283_KM -- P57

2015/01/13--D7-MICRO3_X00_SCH_0113_2015_2130
1, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_SCH_20150113 DC.DSN

2015/01/15--D7-MICRO3_X00_SCH_0115_2015_1100
1, Add cap - CD57,CD58,CD59,CD56 , CD61,CD62,CD60,CD63- 1uF,
CH101,CH111,CH112,CH113,CH114CH115,CH116,CH117 , CH118,CH119,CH120,CH121,CH122,CH123,CH124,CH125 10uF
del CH92,CH93,CH94,CH95,CH99 , CH88,CH89,CH90,CH91,CH100 .1uF
by follow new memory design guide V1.5 -- P76,P78
2, Change the RO126 pull up power to +3P3V_MAIN from +3P3V_AUX for diag led part --P29
3, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_SCH_20150114 DC.DSN

2015/01/15--D7-MICRO3_X00_SCH_0115_2015_1130
1, change CD8,CD29 from 4,7uF to 10uF by follow new memory design guide V1.5 -- P76,P78

2015/01/16--D7-MICRO3_X00_SCH_0116_2015_0930
1, remove the usb charger part -- P56
2, remove the c330,c331 that co-lay with ecap as remove usb charger ic -- P56
3, Add TP_FM_TBT_FORCE_PWR1 , TP_FM_TBT_FORCE_PWR2 , TP_FM_TBT_FORCE_PWR3 , TP_FM_TBT_FORCE_PWR4 ,
TP_FM_TBT_FORCE_PWR5 , TP_FM_TBT_FORCE_PWR6 , TP_FM_TBT_FORCE_PWR7 , TP_FM_TBT_FORCE_PWR8 ,
TP_FM_TBT_FORCE_PWR9 for no usaged GPIO -- P22,23,24
4, change the PCB p/n to 0101AYH01-491-G as RDE request --P46

2015/01/17--D7-MICRO3_X00_SCH_0117_2015_1030
1, change the RO126 from 10K to 1K -- P29
2, re add the c330,c331 that co-lay with ecap --P56
3, Follow crystal HOSONIC suggestion change 25MHZ crystal(XL1) to E5SB25E00000ME
from E5SB25.0000F20M22, CL7 to 27pF from 22pF for CLK performance --P32
2015/01/19--D7-MICRO3_X00_SCH_0119_2015_1030
1, change the RV54,RF70 from 4,7K,8.2K to 10K,16.2K for deratig issue -- P29
2, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_SCH_20150119 DC.DSN

2015/01/20--D7-MICRO3_X00_SCH_0120_2015_2000
1, change BIOS spi rom from 16M to 8M+4M -- P51
2, Follow TPM2.0 HW Recommendations: -- P45
a. GPIO2, GPIO0 pull up to 3V Main
b. VDD1 reserved 3V main

2015/01/21--D7-MICRO3_X00_SCH_0121_2015_1830
1, dummy 4M SPI BIOS ROM component for cost bom, SPI1,SPI1_1,RF75,RF76,RF77,RF78,RF79 -- P51
2, updated the TPM part by following D7-SFF - RF73,RF68,RF74 from 0603 to 0402 -- P45

2015/01/22--D7-MICRO3_X00_SCH_0122_2015_1000B
1, Remove 4M SPI BIOS ROM component for PM request, SPI1,SPI1_1,RF75,RF76,RF77,RF78,RF79 -- P51
2, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_SCH_20150119B DC.DSN
2015/01/23--D7-MICRO3_X00_SCH_0123_2015_1545
1, change the pull up of SPI_IO2/3, R240,R241 -- P51

2015/01/26--D7-MICRO3_X00_SCH_0126_2015_0930
1, dummy the SPI_VDD1 cap , CF27,CF28 by follow SFF TPM page -- P45
2, change the RX140 from 1K to 0 ohm by follow Micro7 in NGFF --P57
3, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X00_SCH_20150122 DC.DSN
2015/01/26--D7-MICRO3_X00_SCH_0126_2015_1530
1, change the PU15 temp p/n follow the SFF --P72

2015/01/27--D7-MICRO3_X00_SCH_0127_2015_1330
1, install R237, dummy R236 as intel MoW03 by follow SFF --P26

2015/01/29--D7-MICRO3_X00_SCH_0129_2015_1650
1, change RX178 to proto, RX177 to NI by follow Micro7 --P57
2, change RH66,RH63 to NI by follow Micro7 --P10
3, change RH73,RH68 to proto, RH74,R57,R91,RH2 to NI by follow Micro7 --P09

X01 change list

2015/03/02--D7-MICRO3_X01_SCH_0302_2015_0930
1, modify the module name by following the Micro7 -- FrontSwitch, DP Header, PCIE 4X, TBT,

2015/04/01--D7-MICRO3_X01_SCH_0401_2015_1430
1, modify the version ID to X01 -- P28
2, TPM vendor's suggestion , for SPI_VDD3, CF18 need close to Pin 22; remove CF19,CF22 ,
for SPI_VDD1, Stuff CF28 , remove CF27, for +3P3V_MAIN, stuff CF25,CF26. -- P45
3, Un stuff R237, stuff R236 (SPI_IO3) by following the MoW06/09 --P26
4, For diag led costdown, add RO130, un stuff Q20,Q19,RO127,RO129,RO126,RV54,RF70 -- P29
5, Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X01_0401_DC-DC.DSN

2015/04/02--D7-MICRO3_X01_SCH_0402_2015_1730
1, Unstaff RL46,QL6 as Lan can't disable -- P32
2, Change the RF41,RF42 from 15ohm to 33ohm by follow PDG1.5 -- P51
3, change CPU ILM cover +BP from PT44A69-6411 to PT44A69-641D,? and change the footprint -- P10

2015/05/06--MICRO3_X01_SCH_0506_2015_1530
1, Change the DIMM2 from ASAA627-H8SB0-7H to ASAA627-H8SB0-4H --P76
2, Change the DIMM1 from ASAA627-N4SB2-7H to ASAA627-N4SB2-4H --P78
3, Change the chipset form 940717 QHPT to 943904 QJP5
4, Change RO112 from 200 Ohm to 1K Ohm,RO86form 470 Ohm to 390 Ohm --P55

2015/05/07--MICRO3_X01_SCH_0507_2015_1500
1, Change 0 Ohm resister to short pad,Location
R10,R11,R14,R51,R154,R108,R97,R113,R106,R93,R94,R112,R95,R110,R62,R347,R353,R263,R107,R111,
R114,R119,R439,R432,R395,R126,R436,R437,R438,R398,R399,R400,R168,RP44,R182,RO93,RO67,RO94,RO119,
RP67,RP68,RP84,RP70,R190,R196,RL61,RL63,RL64,RL65,RF56,RF59,RF48,RF60,RF61,RF53,RO116,RF55,RO20,
RO26,RX148,RX141,RX142,RX143,RX23,RX24,RX146,RX147,RX150 --P10,P11,P14,P22,P23,P24,P26,P29,P39,
P41,P45,P46,P51,P55,P57
2, Remove C322,C323,C324,C325,C326,C327,C328,C329 ,C330,C331 --P43,P56
3, Change USB3.0 CONN from UEA1117-44161-4H to UEA1117-44126-4H -P43,P56
4, , Changing overall DC circuit. --P59~P82 but P76,P78
--D7-MICRO3_X01_0507_DC-DC.DSN
5, Stuff R241 --P51

2015/05/08--MICRO3_X01_SCH_0508_2015_1130
1, Change the C116,C117 form 18pF to 12pF,change the C118,C119 form 22pF to 27pF --P25
2, FAB1 pull up change form +5V_AUX to +5VAUX_LPS_LDO --P34

2015/05/09--MICRO3_X01_SCH_0509_2015_1130
1, Remove RX155,RX156,RX167,QX6,R86,QX3,RX153,QX1,RX154 --P57
2, Update INTRUDER information from CIS database --P28

2015/05/12--MICRO3_X01_SCH_0512_2015_1100
1, MH5, MH6, MH7 footptint change to MH40X80_10_DELL from MH40X80_8_DELL,and change the hole symbol --P54
2, MH1 footptint change to MH_157_394_10_HDD from MH_157_394_8_HDD,and change the hole symbol --P54
3, MH2,MH3,MH4 footptint change to MH_178_394_10_DELL from MH_178_394_8_DELL,and change the hole symbol --P54
4, Delete U26,and location U26_1 change to U26 --P33

2015/05/15--MICRO3_X01_SCH_0515_2015_1400
1, Change RO72 form470 ohm to 499 ohm --P55

2015/05/27--MICRO3_X01_SCH_0527_2015_0920
1,Change USB Connector name to USB3_R,USB4_R form SSUSB3_R,SSUSB4_R --P43
2,Stuff RH56,RH58,R203, Unstuff RH72 For XDP design request -P09,P26
3,Stuff PC80,PC81 meet VCCSA spec --P67
4,update INTRUDER pin SCH --P28
5,Swap SSD_SATA_DEVSLP&WLAN_USB_Detect --P23

2015/06/01--MICRO3_X01_SCH_0601_2015_1640
1,Stuff RF68,unstuff RF74 --P45

2015/06/03--MICRO3_X01_SCH_0603_2015_1530
1,Unstuff R240,241 --P51

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